Errata

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Manual Part Number: 03586-90000

HP References in this Manual

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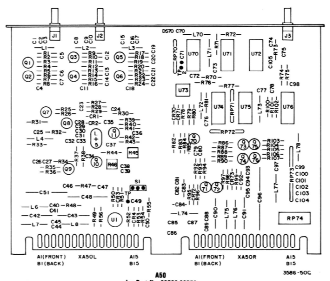

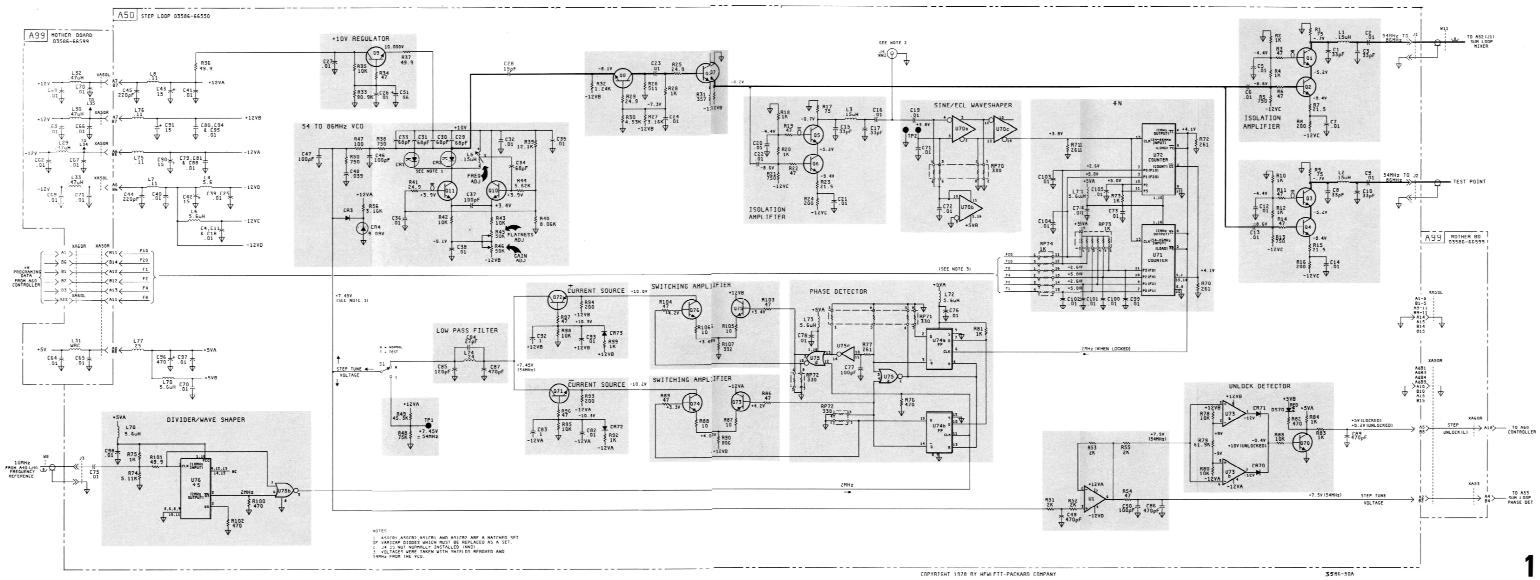

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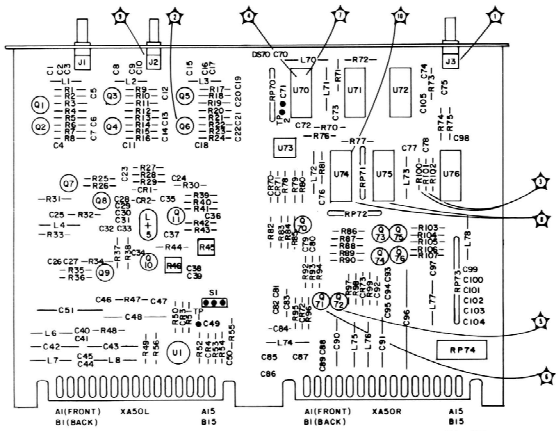
Figure 8-D-3. Schematic Diagram - Step Loop (A50)



NOTES

1. If S1 is switched to TEST, the VCO frequency should be 54 MHz (± 0.1 MHz).

2. If S1 is switched to TEST and TP1 is grounded, the VCO frequency should be approximately 77 MHz.

3. If TP2 is shorted to ground, the 2 MHz output from the counters (U71/U72) should go to zero. The 2 MHz reference from U75(3) may then be followed through the Phase Detector (Paragraph 8-D-19, steps 10 through 13).

4. If TP2 is shorted to ground, the unlock circuit should drive negative at the detector (U73/Q70) and DS70 should light.

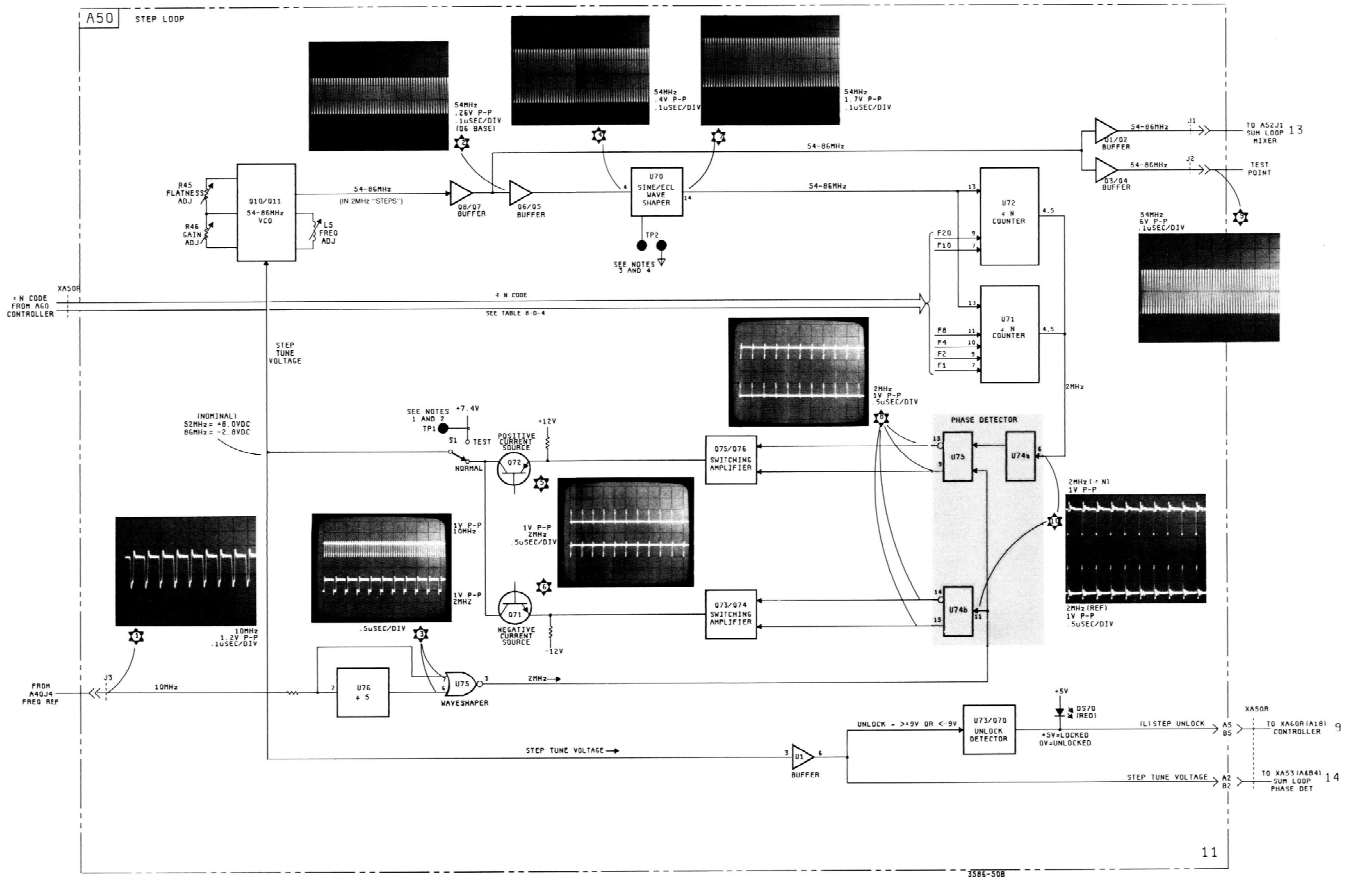


Figure 8-D-4. Functional Block Diagram - Step Loop (A50)
8-D-13/8-D-14

8-D-25. Breaking The Sum Loop.

8-D-26. If the frequency at XA53(B14) is correct and that at XA53(B12) is incorrect, the problem is in the sum loop. Use the following procedure to break the sum loop for troubleshooting.

1. Place A51 on an extender board and set A51S1 to TEST. Put a frequency counter on A51J2. The Sum VCO frequency at A51J2 should be 52MHz (±.1MHz).

2. If it is not 52MHz, check A51J1 and A51J3 to eliminate the Isolation Amplifiers. If it is not 52MHz at any of the outputs and TP1 is about +7.5V, the problem is in the VCO or in Q11. There is no simple way to identify a defective VCO component. Gain what information you can from schematic voltages (Figure 8-D-5) and then replace the VCO active components, one-at-a-time, until the bad component is found.

3. If the loop locks up with S1 in TEST at 52MHz, short A51TP1 to ground. The loop should now lock up at about 75MHz. This allows a look at a frequency other than the TEST frequency. Applying a DC source to A51TP1 (between +8V to −8V) should vary the VCO frequency between 50MHz and at least 82MHz (probably closer to 100MHz) for additional checks. (Remove the short first.)

CAUTION

If a problem exists in the VCO circuit, driving A51TP1 with too much current from a DC source could destroy additional circuit components.

4. If the VCO is working, leave A51S1 in TEST to check the Sum Mixer (A52). Place A52 on an extender. With the tuned frequency at 1MHz, verify the Step VCO input at A52J1 is 54MHz and the Sum VCO input at A52J2 is about 52MHz (TEST frequency). Next check that the mixer output at XA52(A12) is about 2MHz (Step VCO minus Sum VCO). If not, the problem is on A52. Use a scope and Figure 8-D-8 to isolate to a stage on A52.

5. Another way to check A52, if the Sum VCO is not working even in TEST, is to jumper the 50MHz reference from A40J6 to A52J2. If the front panel is tuned to 1MHz, the Step VCO should be 54MHz and the Mixer output should be 4MHz (54-50MHz). If the tuned frequency is then changed to ØHz, CARRIER Measurement mode selected, ENTRY FREQUENCY = TONE, and ↗ (USB) CHANNEL selected, the Step VCO will change to 52MHz and the Mixer output should be 2MHz (52-50MHz).

6. If the mixer output is correct, place A53 on an extender board. Change the tuned frequency on the front panel to 1,999,999Hz. Check that the Fractional-N input to A53 at A53J1 is 2,000,001Hz. If yes, and the A52 mixer output of about 2MHz is also present at XA53(B12), the problem is on A53.

7. If the Fractional-N input at A53J1 is not correct, pull out the A31 board from the instrument. Next, remove the coax cable from A2J3 and A5J1. Connect the coax from A40J2 to A53J1. This will provide the 2MHz frequency reference from A40 as a substitute for the Fractional-N input to the Sum phase detector. Place A51S1 back in NORMAL. If the Sum Loop now locks up by itself at 52MHz as indicated by 2MHz present at XA53(B12) and extinguishing of the Sum "unlock" LED (A53DS1), then the problem is in the Fractional-N

loop. Proceed to Service Group E and continue troubleshooting. If not, then two separate problems exist, one in the Fractional-N loop and one on the A53 board. Proceed to Service Group E to troubleshoot the Fractional-N problem or continue in step 8 for the A53 problem.

8. If the FN input is good and the input from the Sum Mixer is good, but A53DS1 is lit (Sum loop unlocked), remove A53U6 from its socket and ground A53TP2. With U6 removed (killing the 2MHz from A52), the SUM TUNING VOLTAGE at XA53(B2) should drive to about −11V and the Sum VCO frequency (A51S1 in NORMAL) should drive to around 95MHz. If it doesn't, check for the presence of the FN 2MHz at U5(2) and U5(3). If it's there, Q5, Q6, or Q7 are probably bad. If missing, U3, U4, or U5 are probably bad.

9. If the voltage at XA53(B2) is correct (about −11V), check TP1. If it's not about −10V then U2 or U1 are probably bad. Replace U6 in its socket.

10. The remaining potential problem area on A53 involves U1 and U3. To check the comparator outputs to the loop, proceed as follows. Short TP2 to ground. Now short the two pins of TP3 together. This should turn off the Phase Detector by setting the D input LOW. U6(14) and U6(3) should be HIGH (+4.3V). U6(15) and U6(2) should be LOW (+3.3V). The NEGATIVE current source (Q5) should be on and the POSITIVE current source (Q4) should be off. Q2 and Q6 should be off. Q3 and Q7 should be on. The SUM TUNING VOLTAGE at XA53(B2) should be full negative (about −11.7V) and the Sum VCO should be at about 96MHz (A51S1 in NORMAL). DS1 should be lit.

11. Remove the short from TP3. Short the two pins of TP4 together. The following conditions should now exist. U6(15) and U6(3) should be HIGH. U6(14) and U6(2) should be LOW. The POSITIVE current source (Q4) should be on and the NEGATIVE current source (Q5) should be off. Q2 and Q6 should be on. Q3 and Q7 should be off. The SUM TUNING VOLTAGE should be full positive (about +11.4V) and the Sum VCO should be at about 36MHz. DS1 should be lit.

12. If the conditions in both step 10 and step 11 are correct, then U1 or U3 are probably bad. Remove the shorts from TP2 and TP4. Connect a DC source to TP2. When the voltage at TP2 is held between +1.8V and −.6V, DS1 should not be lit. If it is, U3 is probably bad. Changing the voltage at TP2 above +1.8V or below −.6V should cause the comparators to trip and DS1 to be lit. If they do not, U3 is probably bad. If U3 works correctly, the problem must be U1 bad.

8-D-27. Sum Loop Hints.

8-D-28. If the regulated +10V on A51 is higher than +10V *and* the SUM TUNING VOLTAGE is higher than +10V, the regulator might be good. Put A51S1 in TEST to force the tuning voltage to +7.5V. If the regulated +10V drops to +10V, the regulator is operating normally.

8-D-29. When the Sum loop is malfunctioning and a good First L.O. signal is needed to test other parts of the instrument, it is possible to provide a temporary substitute First L.O. Lift one end of A51L6 and inject a variable frequency source from 50-82.5MHz directly into A51J4. Set the source amplitude to −40dBm (75 ohm output impedance). With a second source into the front end (A1) and a counter on the Second I.F. test jack (15.625KHz-IFTP) on A10, the whole frequency conversion section of the receiver can be exercised. Use a full

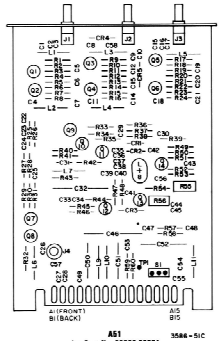
scale input signal to A1 and be sure all your test instruments are phase locked together for accurate frequency measurements.

8-D-30. A53 Adjustment Note. When adjusting A53R3 (GAIN) and A53R13 (OFFSET), be sure to monitor the Sum VCO frequency. The loop can be locked up to the wrong frequency with these adjustments. Follow the procedures in paragraph 5-6 carefully, remembering that the Sum VCO should be equal to the front panel tuned frequency (plus 50MHz) in LO DIST or LO NOISE.

8-D-31. Post-Repair Adjustments (A50/A51/A52/A53).

8-D-32. After any repairs to the current sources, current switches, or Sum/Step VCO's, check for the presence of spurs (paragraphs 4-37 and 4-39).

8-D-33. After replacement of the matched set of VARICAP tuning diodes on A50 and A51, perform *all* Sum and Step Loop adjustment procedures (paragraph 5-6).



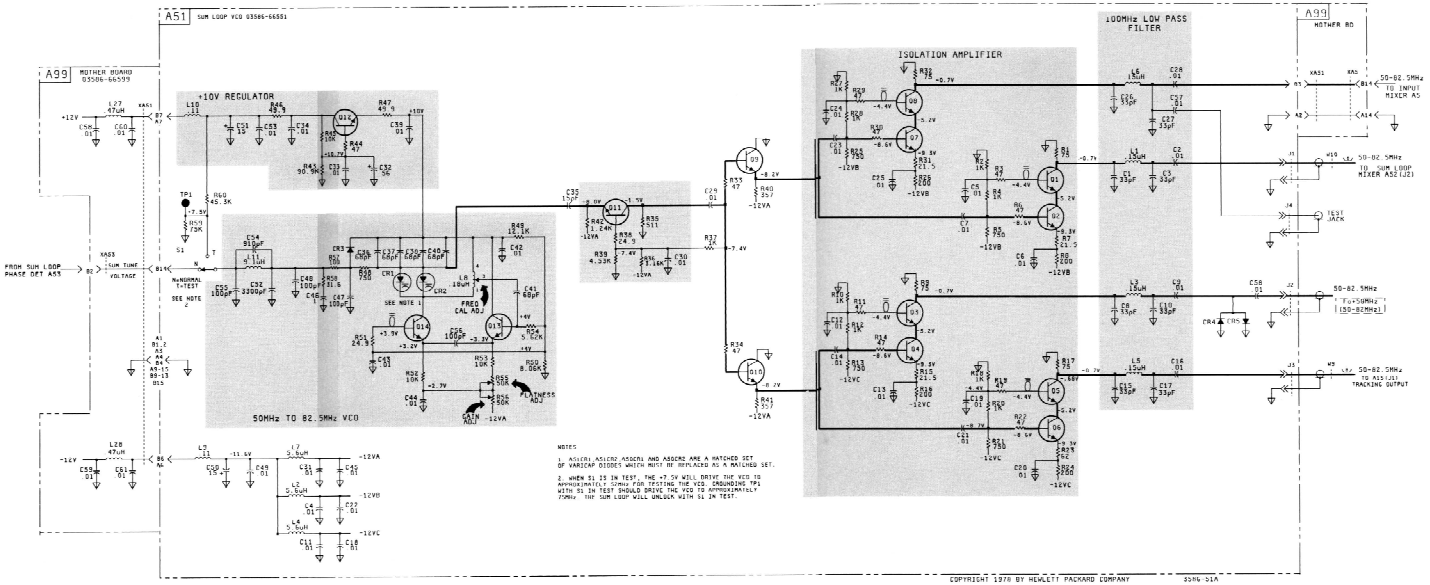


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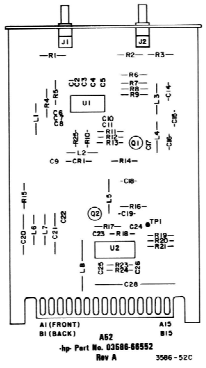
Figure 8-D-5. Schematic Diagram - Sum Loop VCO (A51)



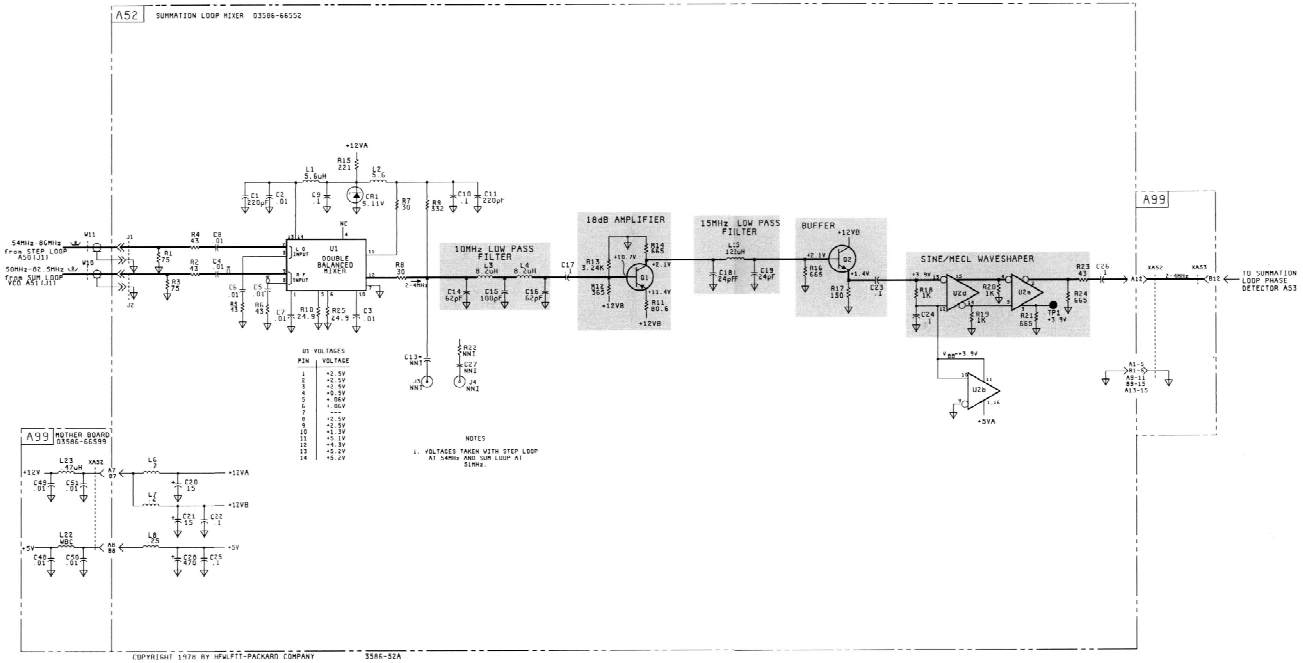
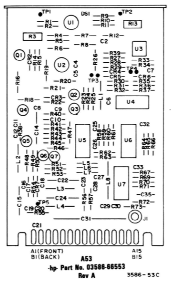


Figure 8-D-6. Schematic Diagram - Sum Loop Mixer (A52)



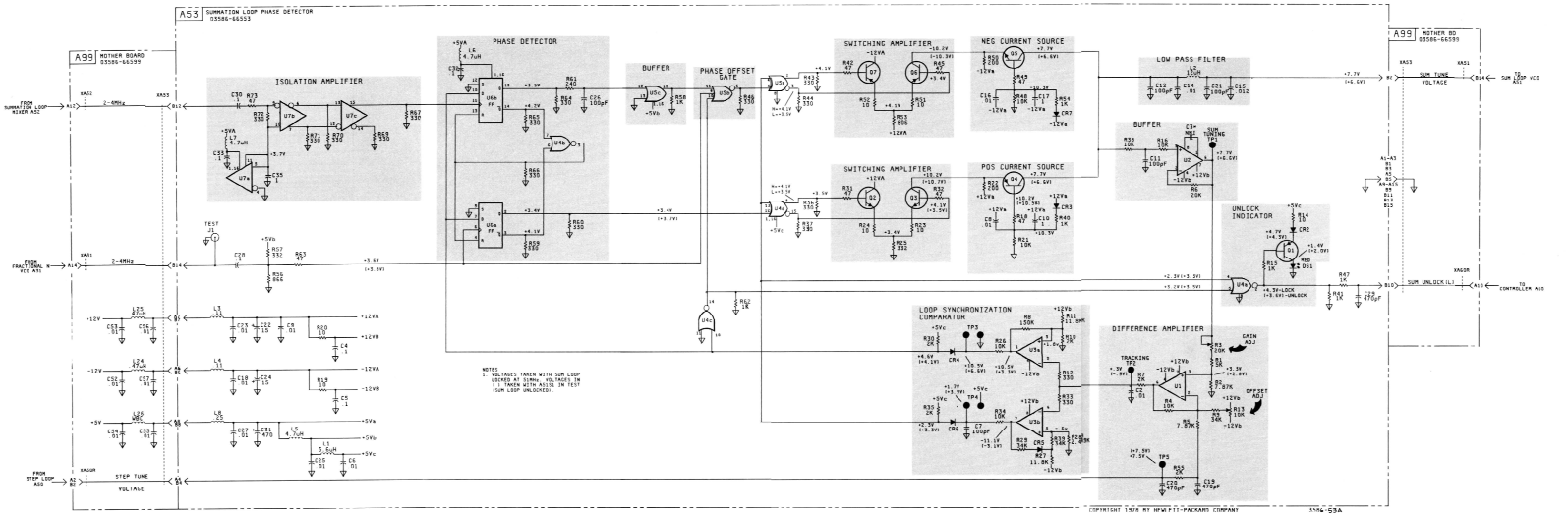
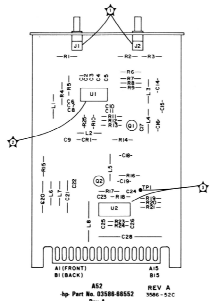
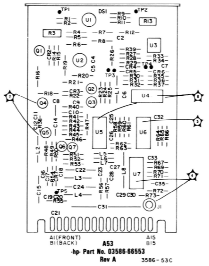
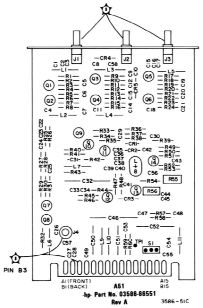


Figure 8-D-7. Schematic Diagram - Sum Loop Phase Detector (A53)







NOTES

1. Voltages and waveforms were obtained with the front panel tuned to 1 MHz. The First L.O. frequency is then 51 MHz (SUM VCO output) and the Step Loop VCO frequency is 54 MHz. The two signals entering phase detector A53U6 should therefore be 3 MHz (54-51).

2. All voltages are + or - 10% unless otherwise noted.

3. The 2 MHz reference from A40J2 may be jumpered to A53J1 for test purposes with A31 removed. Refer to Paragraph 8-D-26, step 7, for information.

4. Test A: With A53TP2 shorted to ground and a jumper across the dual pins of A53TP3, A53TP1 should be -9.7v (± 1.2v).

   Test B: With A53TP2 shorted to ground and a jumper across the dual pins of A53TP4, A53TP1 should be +11.0v (± 1v).

5. A53U6 is in a socket for easy removal during trouble shooting. This allows signal tracing of the FN 2-4 MHz signal. Refer to paragraph 8-D-26, step 8, for information.

6. With A51S1 in TEST, the SUM VCO should be 52 MHz (± 0.1 MHz). If A51TP1 is then grounded, the SUM VCO should drive to approximately 75 MHz.

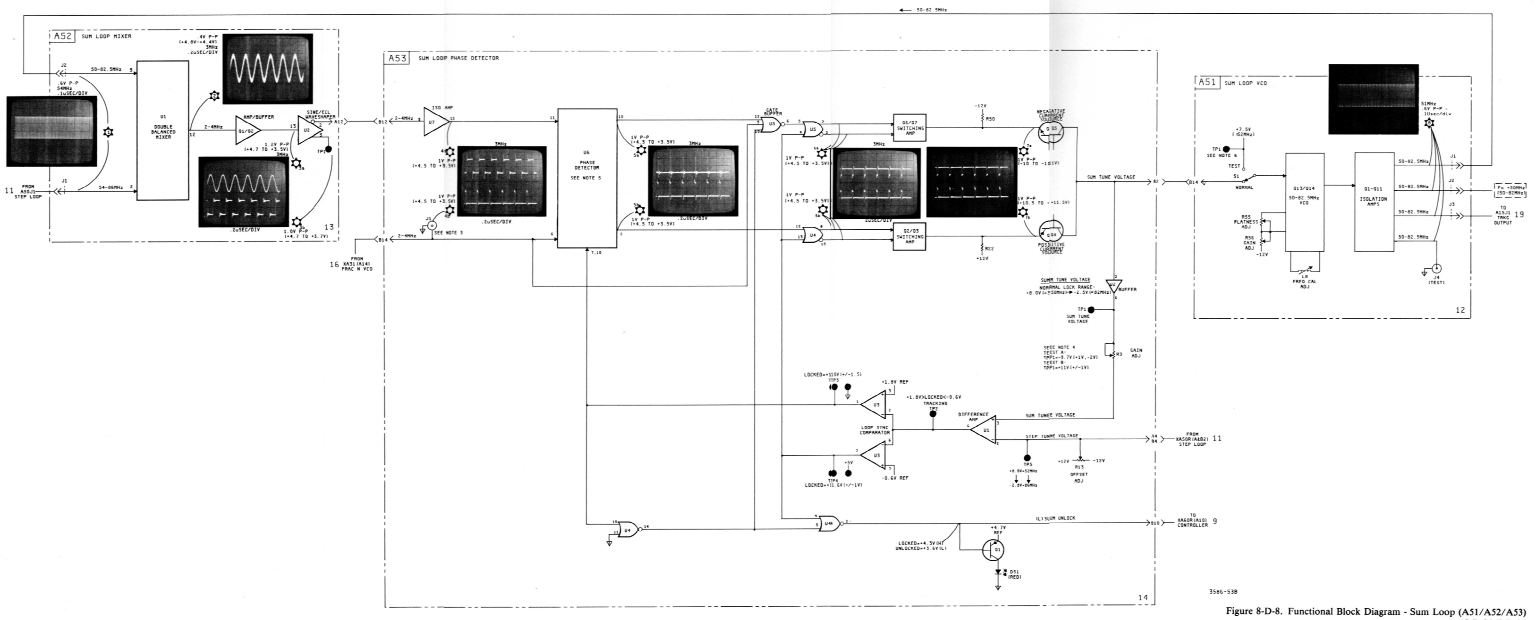


Figure 8-D-8. Functional Block Diagram - Sum Loop (A51/A52/A53)

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FRACTIONAL-N
SERVICE GROUP E

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8-E-1. ADJUSTMENTS (CROSS REFERENCE).

8-E-2. FN VCO Adjustments (A31).

Designation	Adjustment Title	Paragraph
A31L4	Oscillator Frequency Adjust	5-5
A31R4	Tune Voltage Gain Adjust	5-5

8-E-3. FN Phase Detector Adjustments (A32).

Designation	Adjustment Title	Paragraph
A32R51	API-1 Adjust	5-5
A32R54	API-2 Adjust	5-5
A32R61	API-4 Adjust	5-5

8-E-4. THEORY OF OPERATION (CROSS REFERENCE).

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8-E-8. Fractional-N ÷ N (A30) - Paragraph 8-233.

8-E-9. TROUBLESHOOTING DATA.

8-E-10. Verifying a Fractional-N Problem.

8-E-11. Before attempting to troubleshoot the Fractional-N loop, verify that a problem does exist as follows.

1. Place A31 board on an extender card.

2. Connect a frequency counter to XA31(A14).

3. Apply power to the 3586 or press RECALL and Ø to establish turn-on conditions.

4. Tune the 3586 to each one of the frequency values in Table 8-E-1, verifying the FN VCO (÷ 10) frequency at XA31(A14). If all frequency read outs on the counter are correct for the tuned frequencies in the table, proceed with step 5. If any of the frequency readouts are incorrect, proceed to paragraph 8-E-15.

5. If the frequencies at XA31(A14) are correct per Table 8-E-1, connect a scope to XA31(A14). The signal at that point should be about 1Vp-p around a zero reference, and should be a pulse about 15 to 30 nanoseconds wide (pulse width depends on frequency). If not, troubleshoot A31 using Figure 8-E-6 and Figure 8-E-4.

6. If the frequency, waveform and amplitude are all correct at XA31(A14) for the values in Table 8-E-1, the Fractional-N loop is working correctly. Proceed to Service Group D and troubleshoot the Step and Sum Loops if the First L.O. signal is the incorrect frequency.

8-E-12. Error Code E3.4.

8-E-13. Whenever error code E3.4 is displayed on the front panel, it indicates that an "unlock" condition exists for the FN loop. Determination of unlock is made by a detector circuit (U2/Q9) which checks the FN TUNE voltage continuously to see if it is greater than +8.6V or less than −8.6V. If yes, one-half of U2 trips high, turning on Q9 and sending a (L) FN UNLOCK signal to the processor which displays the error code.

Table 8-E-1. FN Codes and Frequencies.

Front Panel Tuned Frequency	FN VCO Frequency at A31TP1	FN VCO ÷10 at XA31 (A14)	÷N Code	Counter Preset Code (÷N Nines Complement)												Decimal Preset Code
				U1 Pins (MSD)				U2 Pins				U3 Pins (LSD)				
				11(D)	3(C)	10(B)	4(A)	11(D)	3(C)	10(B)	4(A)	11(D)	3(C)	10(B)	4(A)	
1,000,000.0Hz	30,000,000Hz	3,000,000.0Hz	300	0	1	1	0	1	0	0	1	1	0	0	1	699
1,000,000.1Hz	29,999,999Hz	2,999,999.9Hz	299	0	1	1	1	0	0	0	0	0	0	0	0	700
1,111,111.2Hz	28,888,888Hz	2,888,888.8Hz	288	0	1	1	1	0	0	0	1	0	0	0	1	711
1,222,222.3Hz	27,777,777Hz	2,777,777.7Hz	277	0	1	1	1	0	0	1	0	0	0	1	0	722
1,333,333.4Hz	26,666,666Hz	2,666,666.6Hz	266	0	1	1	1	0	0	1	1	0	0	1	1	733
1,444,444.5Hz	25,555,555Hz	2,555,555.5Hz	255	0	1	1	1	0	1	0	0	0	1	0	0	744
1,555,555.6Hz	24,444,444Hz	2,444,444.4Hz	244	0	1	1	1	0	1	0	1	0	1	0	1	755
1,666,666.7Hz	23,333,333Hz	2,333,333.3Hz	233	0	1	1	1	0	1	1	0	0	1	1	0	766
1,777,777.8Hz	22,222,222Hz	2,222,222.2Hz	222	0	1	1	1	0	1	1	1	0	1	1	1	777
1,888,888.9Hz	21,111,111Hz	2,111,111.1Hz	211	0	1	1	1	1	0	0	0	1	0	0	0	788
2,000,000.0Hz	40,000,000Hz	4,000,000.0Hz	400	0	1	0	1	1	0	0	1	1	0	0	1	599

Notes: 1. 0 = +0.2 VDC
1 = +4.4 VDC

2. The table values shown will repeat for every 2MHz increment that is added to the Front Panel Tuned Frequency.

8-E-14. If E3.4 is displayed, check the FN TUNE voltage at A31TP3. It should always be between ØV (FN VCO at 40MHz) and +6V (FN VCO at 20MHz). If it is between ØV and +6V, U2 or Q9 are probably bad. If the FN TUNE voltage is > +8.6V or < −8.6V, proceed to paragraph 8-E-17.

8-E-15. FN Loop Locked at Wrong Frequency.

8-E-16. If the FN Loop is locked up (no error code E3.4 displayed), but the incorrect frequency is present at XA31(A14), at TP2, or at A31TP1 per Table 8-E-1, it is possible that the incorrect ÷N code is being received at the FN Logic Chip (A30U16) from the processor. Proceed as follows.

1. Place A30 on an extender board.

2. Press RECALL and Ø to restore turn-on conditions.

3. Check the voltage at U16 pins 20-23. They should all be about +0.3V (LOW).

4. Connect a scope to each pin (20 through 23) of U16, one-at-a-time, while commanding a frequency change using the FREQ STEP function of the RPG (FREQUENCY TUNE knob). You should be able to see the new ÷N codes from the A60 processor causing very short pulses (<.1μS) on each line *only* while turning the RPG knob. You may have to turn your sweep intensity up high and your sweep speed down very slow on your scope to see the pulses because of their narrow width. A pulse-catcher of some sort may also be used.

5. If the pulses from A60 are not present at the input to A30U16, proceed to Service Group C and troubleshoot A60. If they are present, check to see if the correct ÷N code is getting to the decade counters (U1, U2, U3) as follows.

6. Press RECALL and Ø. Tune the 3586 to each one of the frequency values in Table 8-E-1 and check the BCD code at the preset input to U1 (MSD), U2, and U3 (LSD). If the problem appears to be frequency-related, it is best to check all of the frequency codes in Table 8-E-1 as this sometimes can isolate the problem to a particular line or to a couple of components. If all frequencies are bad, only one or two codes need to be checked to see if the preset data is getting to the decade counters at all.

7. If the correct code is not showing up at the decade counters, suspect U9, U10 and U16. Using the RPG as in Step 4, check for the output lines of U16 (pins 13-16) to be pulsing.

8. If the correct codes are getting to the decade counters, use standard digital troubleshooting techniques to check the clocks, inputs and outputs of the flip-flops, gates, and decade counters until the bad IC chip is found. Follow the VCO input through the board and use Figure 8-E-6 to verify signal flow and waveshapes where possible.

8-E-17. Breaking The Fractional-N Loop.

8-E-18. As in all phase-locked loops, the first troubleshooting step is to verify VCO operation. Then work your way around the loop (Figure 8-E-1) until the problem is isolated. Proceed as follows.

1. Place A31 on an extender board and short A31TP3 to ground. This should cause the VCO to oscillate at about 40MHz (A31TP1). If it does not, the VCO has a problem. Check

U1(1) for about −8V to −9V with TP3 shorted. If present, U1 is probably good.

2. If the oscillator is not running at all with TP3 shorted, suspect CR4-CR6, Q1 and Q2 first. Make sure Q3 is not shorted. Make what measurements you can from the schematic (Figure 8-E-4) and then replace the active components one-at-a-time until the bad component is found. Q1 and Q2 should be on at all times.

3. If the oscillator is running, leave TP3 shorted and check all of the A31 board outputs using a scope. If absent from any one output, trace the signal backwards until the bad stage is found.

4. If the VCO output to the A30 board is present and at the correct frequency (about 40MHz with TP3 shorted), the A31 board is probably working correctly. Removing the short to ground and jumping A31TP3 to the +5V supply at either end of L3 should yield another test frequency from the FN VCO of about 22 MHz.

5. Place A30 on an extender board and verify the VCO input at A30TP1 is about 40MHz with A31TP3 shorted to ground. If present, tune the 3586 to 2MHz and then check A30TP3 for the presence of a 100kHz, very narrow pulse signal at about 2Vp-p. If present, the A30 board is probably good. Proceed to step 7.

6. If the 100kHz pulse is missing at A30TP3, follow the steps in paragraph 8-E-16 to check out the A30 board.

7. If the 100kHz pulse is present at A30TP3, put A30 and A31 back in their slots and place A32 on an extender board. *Leave the short on A31TP3.*

8. The best tool for troubleshooting the A32 Fractional-N Phase Detector board is a good understanding of how the board functions. If time permits, read the theory of operation for A32 in paragraph 8-226.

9. Check the two 100kHz inputs to A32 at TP3 and TP4. If the signal at TP3 is missing, proceed to Service Group H and troubleshoot the 100kHz output from the A40 board. If A30TP3 had the FN÷N 100kHz signal present, A32TP4 should have it also.

10. Next check TP8 for a 100kHz signal as shown in Figure 8-E-6. This signal will be unstable with the loop unlocked but should be present and at the correct DC level (+1.3V to −1.0V) as seen on a scope. The same is true for the other waveforms shown on Figure 8-E-6 which are phase detector-related. They are unstable with the loop unlocked, and some may have different levels than those shown. However, if 100kHz signals are present at TP3 and TP4, the signals at TP8, TP6, and TP2 should be present. Their absence indicates a problem in that general area or preceeding it.

11. The LATCH CLOCK (XA32(A8)), BIAS (TP5), and S+H(TP7) signals should always be present as shown *and should be stable.* API 1-5 should always have a stable 100kHz pulse at 5Vp-p (+5V to ØV) present at the outputs of latches U2 and U3. If any of the signals mentioned in this step are missing, trace them back to their common source (A30U16).

12. Press RECALL and Ø. Connect the scope to A32TP2 (the Integrator output). The signal there should resemble that shown on Figure 8-E-6. Activate the FREQ STEP function of the RPG. Changing the tuned frequency by a few Hertz with the RPG should cause the

ramp-down slope to vary. If it does, basic API current sink operation is working. This indicates that the FN Logic chip (A30U16) is functional and is sending commands to A32.

13. Using the FREQ STEP key in the ENTRY key group, change the Frequency Step to 100kHz. Again using the RPG, vary the tuned frequency from 0Hz to 2MHz while observing the scope connected to TP2. The width of the top flat portion of the integrator output signal should smoothly narrow from approximately 6 microseconds at 0Hz to about 3 microseconds at 1.9MHz and then jump back to 6 microseconds at 2MHz. This sequence should repeat smoothly over each 2MHz segment increment from 2MHz to 32MHz. If it does, then the integrator, the phase detector, the latches, the Bias current circuits, and the overall timing of signals from A30U16 are probably correct.

14. Next, check the FN TUNE voltage at A32TP1. It should agree with the DC level on the scope for the top of the ramp on the integrator output signal at A32TP2. If not, the problem is probably in the Sample/Hold Circuit. If the 100kHz pulse at TP7 is present, suspect Q32-Q34 and U7.

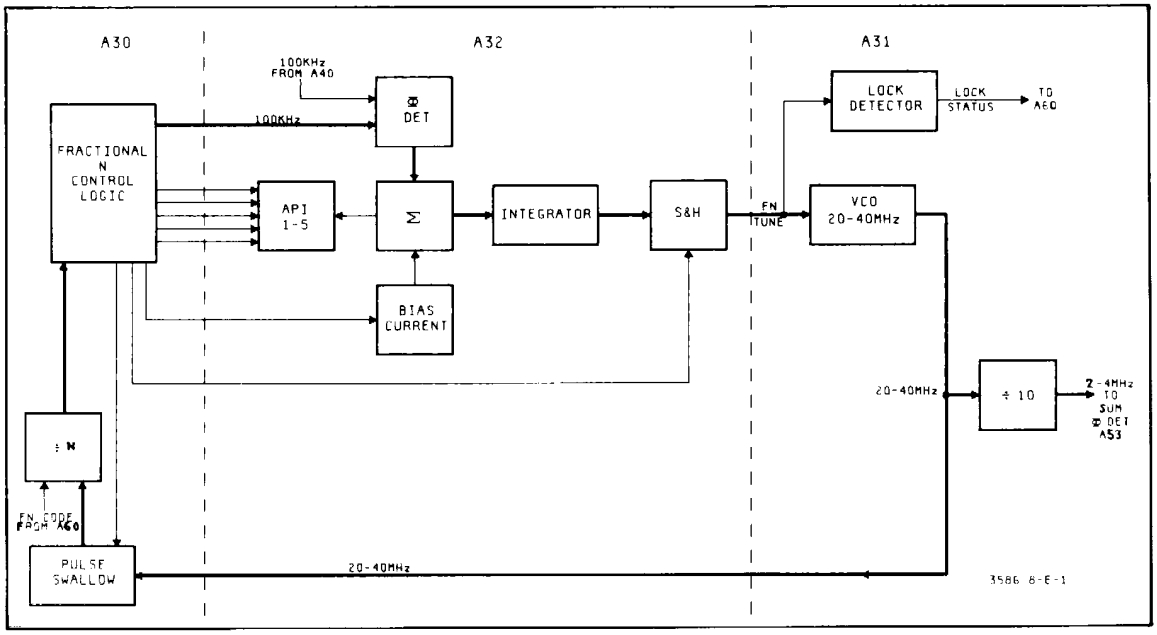


Figure 8-E-1. Fractional-N Loop (Simplified).

8-E-19. Fractional-N Troubleshooting Hints.

8-E-20. As mentioned in a preceding paragraph, the best tool for troubleshooting the Fractional-N loop is a good understanding of how it works. The service technician who has never seen a Fractional-N circuit before should read all of the theory in paragraphs 8-222 through 8-243 before attempting to troubleshoot the loop. Study Figure 8-E-2 and 8-E-6 until a good understanding of functional operation is obtained and then follow the procedure in paragraph 8-E-10 to verify the problem. Review the following hints for additional information that may be of some help.

1. To check the API's, scope the indicated points in Table 8-E-2 while varying the frequency about 2MHz (at the indicated Frequency Step) with the RPG. Use a sweep speed of about 2μSEC/DIV. You should be able to clearly see the narrow API pulses (0-9) in between the wider 100kHz pulses switching in number as the frequency changes. If so, that API is probably working correctly.

Table 8-E-2. API Test Points.

API	Test Point	Freq Step	Amplitude
1	Q18(E)	1kHz	1.5Vp-p
2	Q19(E)	100 Hz	1.0Vp-p
3	Q20(E)	10 Hz	1.0Vp-p
4	U3(5)	1 Hz	3.5Vp-p
5	U3(12)	.1 Hz	5.0Vp-p

2. To check the Unlock Detector on A31 quickly, ground A31TP3. The (L) FN UNLOCK line should be HIGH and LED A31CR11 should be dark. Remove the ground and jumper A31TP3 to either side of L1 (+12V). (L) FN UNLOCK should now be LOW and CR11 should be lit. Move the jumper from L1 to L2 (−12V). (L) FN UNLOCK should again be LOW and CR11 should be lit. Remove the jumper.

3. If the FN VCO oscillates at some frequencies but not others, suspect A31CR4-CR6.

4. Spurious signals at 100kHz coming from the Fractional-N could be caused by a leaky diode A32CR3-CR6. Lift one end of each and check for *at least* 1 Megohm. Make sure they're not open either. Other spurs are possible from out-of-tolerance resistors in U6 although field failures of that precision resistor network are unlikely.

5. For problems that are difficult to isolate, check that the +5V summing node at Q11(s) or U6(2) really is about +5.2V. If not, suspect Q8, Q10, Q11 and Q21.

6. The A32 board is more sensitive than the average board to surface contamination because of the precision currents used to control the FN VCO frequency. Corrosion buildup due to long periods of high humidity, dirt, etc. can cause unusual spurs and unstable operation of the FN Loop. After washing boards to remove dirt, inspect A32 for particles knocked loose which might wedge between IC pins, etc.

7. To check the integrator amplifier operation on A32, lift one end of TL1 at the input to Q22A and jumper Q22A (gate) to TP2. If the amplifier is good, Q30(E) should be ØV. If Sample/Hold is working, TP1 should also have ØV. Replace TL1.

8. If the integrator output at A32TP2 is stuck at the positive rail (+12V), something is pulling too much current out of the integrator input through CR4. If stuck at the negative rail (−12V), something is putting too much current into the integrator.

9. *Always* be sure the FN VCO is running as the first step to checking Fractional-N operation.

10. To check the phase detector circuit on A32, trigger your scope on TP3 and check TP8 for a rising edge. Then, trigger your scope on TP4 and check TP8 for a falling edge. If the indications at TP8 are correct, the phase detector is probably good.

11. If the FN Loop appears to be locked up at the correct frequency, but there is no 2-4MHz input on A53 from the FN loop, trace the signal forward from buffer A31Q7/Q8 to XA31(A14) until it is lost.

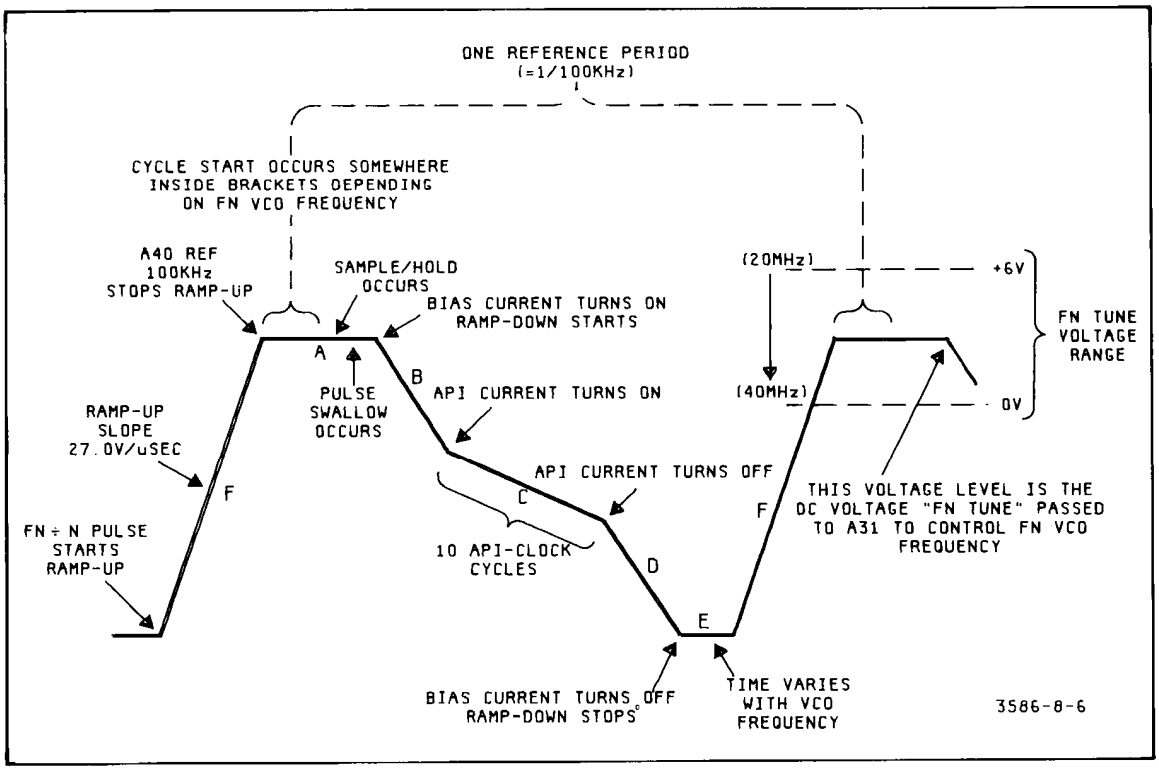
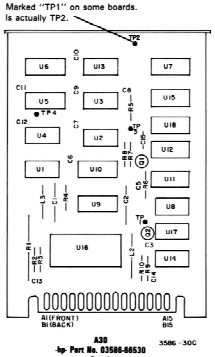


Figure 8-E-2. Fractional-N Integrator Output (A32TP2).



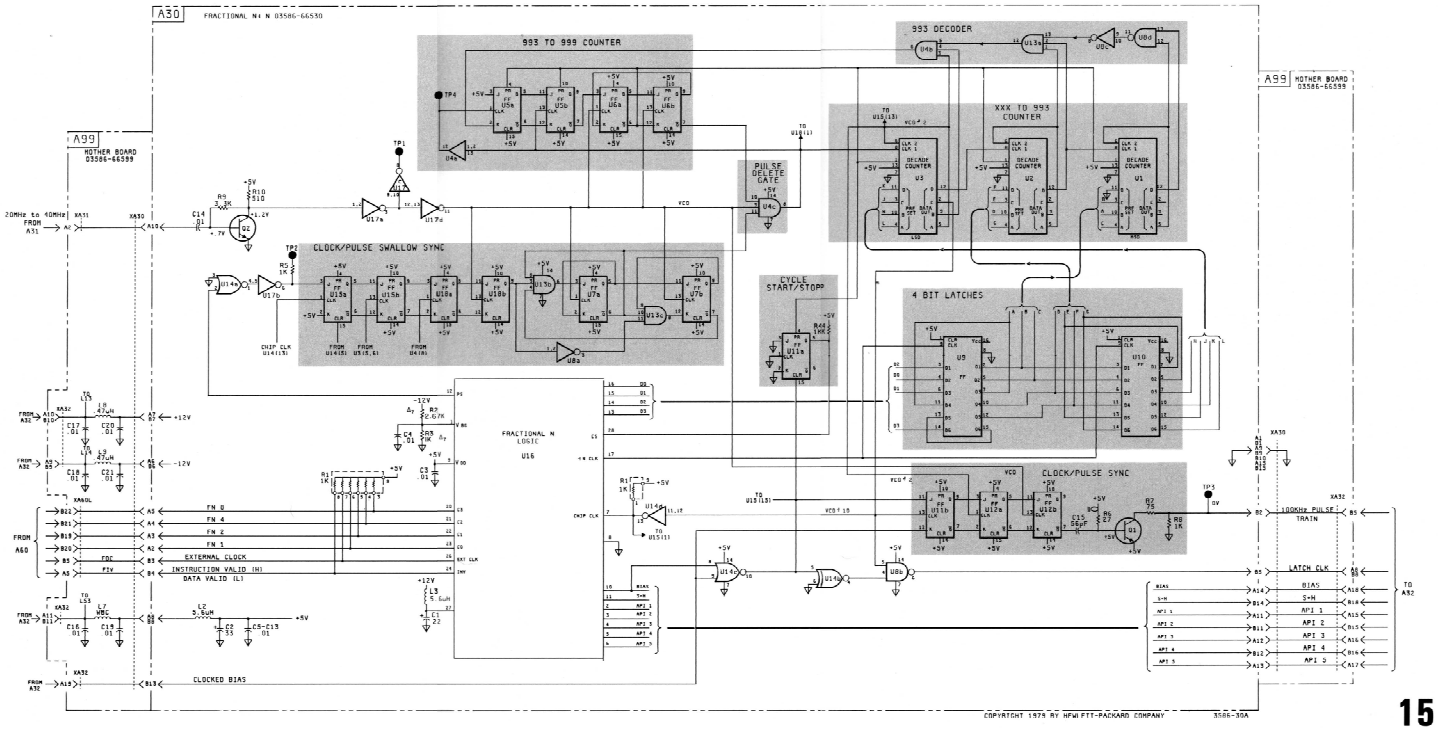
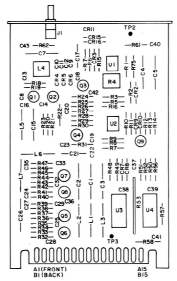


Figure 8-E-3. Schematic - Fractional-N ÷N (A30)



A31
Part No. 03586-66531
Rev A

3586-31C

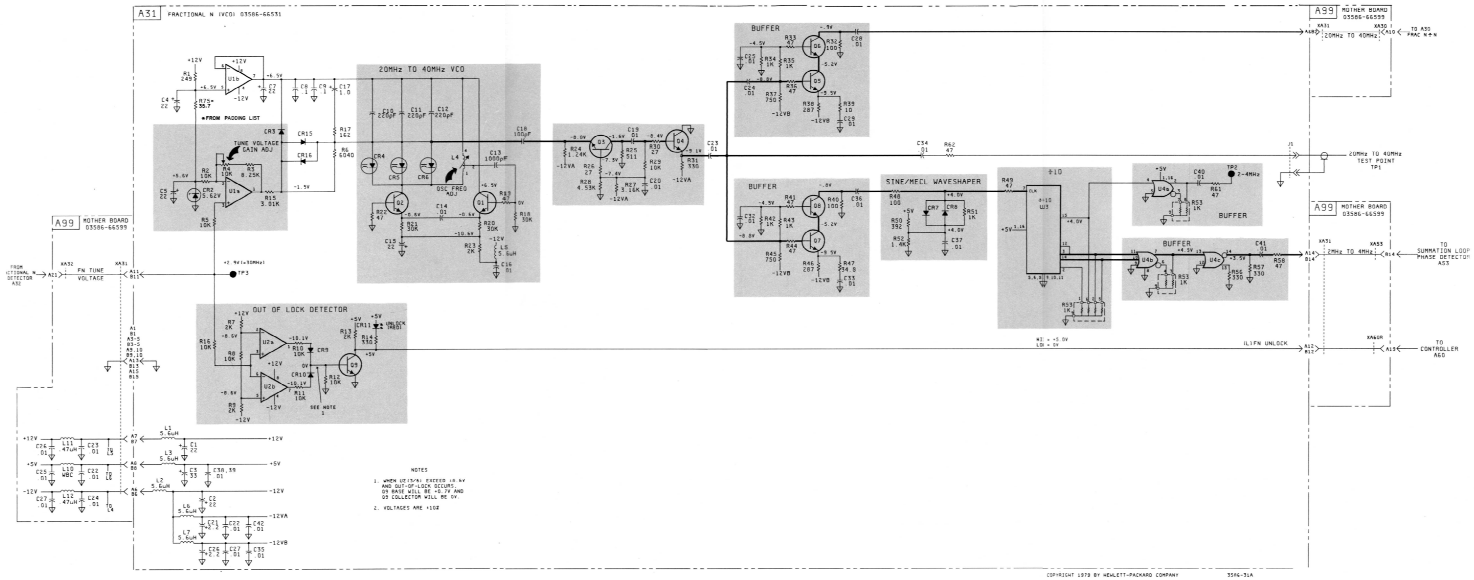


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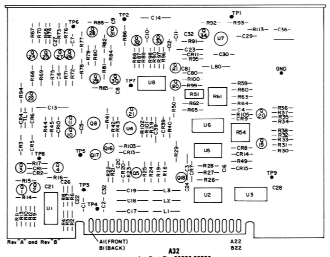
Figure 8-E-4. Schematic - Fractional-N VCO (A31)



NOTES:
1. Voltages were obtained with front panel tuned to 1MHz.
+2.9V at TP1 drives the FN VCO frequency to 30MHz.

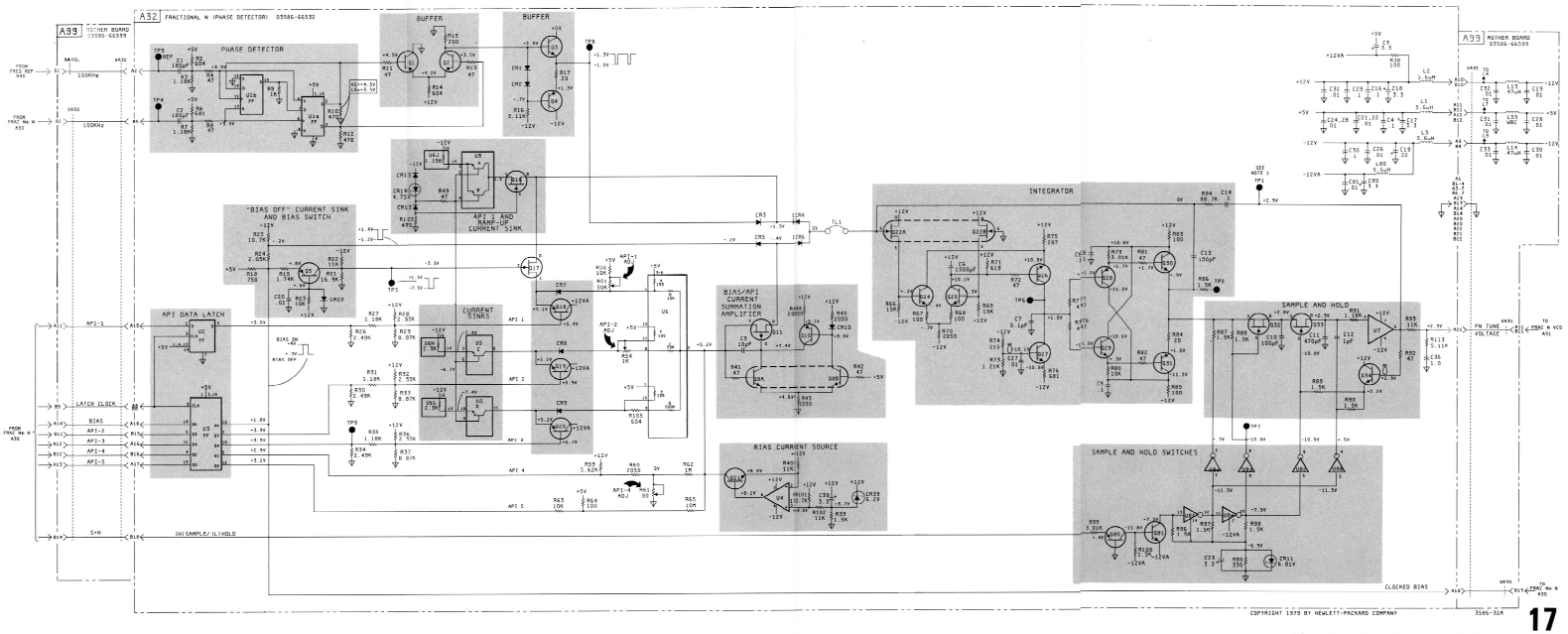
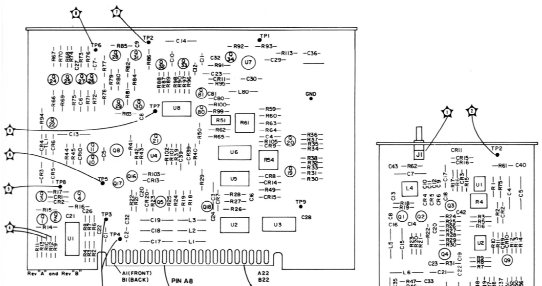


Figure 8-E-5. Schematic - Fractional-N Phase Detector (A32)



NOTES:

1. API 1-5 are active LOW. When BIAS is HIGH and API 1 is HIGH, Q17 and Q18 are on, and CR7 is off. When API-1 goes LOW, Q18 turns off and CR7 turns on, pulling current out of the +5V NODE input to the SUM AMP (QB/Q10/Q11). This causes the integrator ramp-down to shallow out, resulting in an increase of the FN TUNE voltage and a lowering of the FN VCO frequency. Refer to Figure 8-E-2.
2. References to current flow directions on A32 (A-F) may be found on Figure 8-E-2.
3. Tuned frequency must be set to 1,000,000.1Hz for viewing pulse swallow at TP2 and TP4. All other waveforms and frequencies were obtained with the tuned frequency set at 1MHz (FN VCO at 30MHz).
4. TL1 is a 0 ohm resistor that can be removed for checking the integrator. With TL1 removed and a jumper connected from the integrator side of the TL1 sockets to TP2, TP2 should read 0 VDC. If the SAMPLE/HOLD circuit is working, TP1 should then also read 0 VDC.

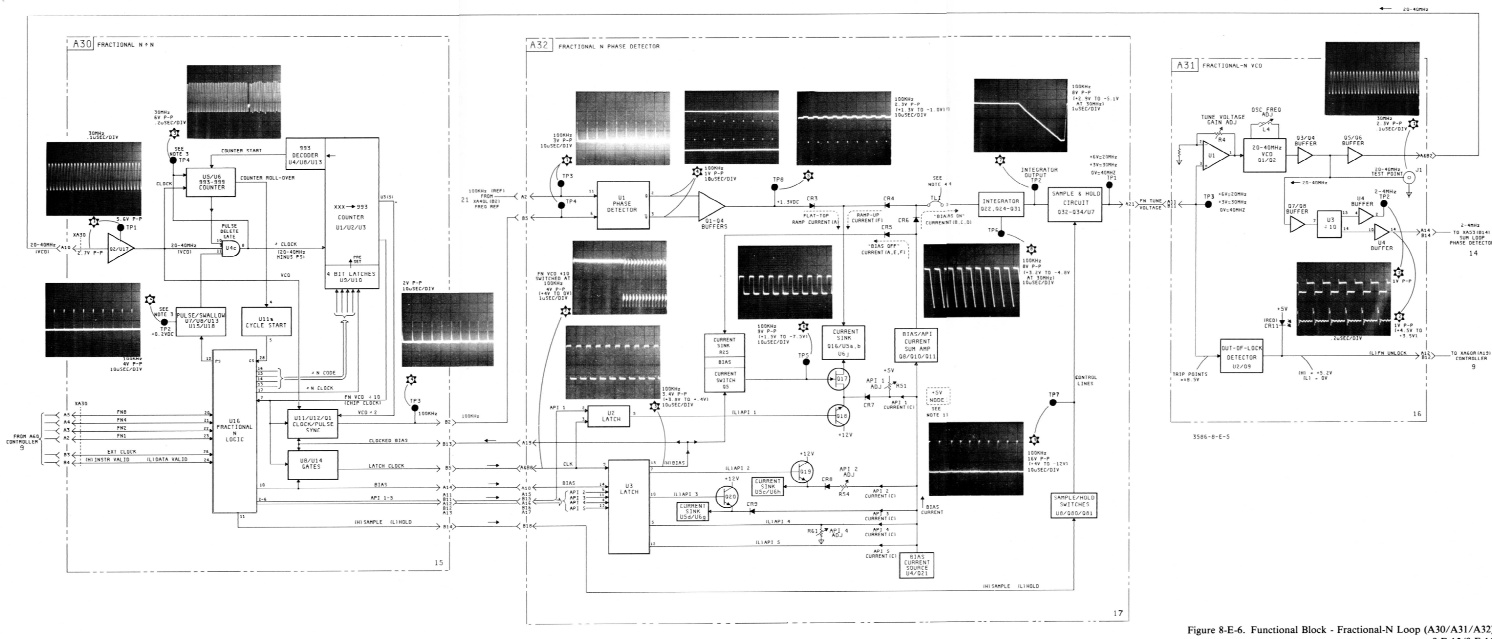


Figure 8-E-6. Functional Block - Fractional-N Loop (A30/A31/A32)

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CALIBRATOR, BROADBAND POWER DETECTOR AND TRACKING OUTPUT SERVICE GROUP F

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8-F-1. ADJUSTMENTS (CROSS REFERENCE).

8-F-2. BBP/OVLD/CAL (A4) Adjustments.

Designation	Adjustment Title	Paragraph
A4C113	−40dBm CAL Flatness	5-20
A4L106	−20dBm CAL Flatness	5-20
A4R24	BBP Flatness Adjust	5-20
A4R29	BBP Offset Adjust	5-20
A4R30	BBP Gain Adjust	5-20
A4R134	−40dBm CAL Level Adjust	5-20
A4R136	−20dBm CAL Level Adjust	5-20

8-F-3. Tracking Output (A15) Adjustments.

Designation	Adjustment Title	Paragraph
A15R3	Mixer Balance Adjust	5-21

8-F-4. THEORY OF OPERATION (CROSS REFERENCE).

8-F-5. BBP/OVLD/CAL (A4) - Paragraph 8-183.

8-F-6. Tracking Output (A15) - Paragraph 8-192.

8-F-7. TROUBLESHOOTING DATA.

8-F-8. BBP/OVLD/CAL (A4) Troubleshooting.

8-F-9. General. Problems related to the A4 board may include intermittent or continuous auto-ranging, WIDEBAND power amplitude measurement inaccuracies, intermittent or continuous underload or overload indications, and several different types of calibration problems. Descriptions of most of these problems together with some general procedures to follow for isolating them are contained in Table 8-9 (Troubleshooting Hints). The service technician should read all of the information under the appropriate general heading for the type of problem indicated (see paragraph 8-91). Included below are some additional hints and information.

8-F-10. Auto-Ranging Problems.

8-F-11. In AUTO 10 or AUTO 100, the 3586 "auto-ranges" when the A60 Controller sees either the UNDERLOAD or OVERLOAD line from the A4 board go high. This signifies that the input to the True RMS Detector/Logger (A4U4) is outside the linear operating range of the chip, as sensed by the Underload/Overload Detector. In response, the processor on A60 will send a command to the A2 board to attenuate the input signal by 5dB (overload condition existing) or amplify the input by 5dB (underload condition). After the command is issued, the processor again samples the UNDERLOAD/OVERLOAD lines. If the condition still exists, another 5dB change is commanded. This sequence continues until both UNDERLOAD/OVERLOAD lines are LOW. At that time, the processor checks the IF signal amplitude and changes IF Gain up or down as required to satisfy the IF Detector /Logger circuit on A21.

8-F-12. If either of the UNDERLOAD/OVERLOAD lines is always HIGH, or if both lines alternate back and forth HIGH to LOW, LOW to HIGH, an auto-ranging problem exists. Possible causes include:

1. An unstable power level on the input signal.

2. Undesired amplitude modulation riding on the input signal or a second signal (undesired and unstable) present at the input.

3. Amplitude modulation of the input signal *by the 3586*, either by the A2 board or by the A4 board.

4. Failure of the A2 circuits to attenuate or amplify the input signal as commanded by the A60.

5. Failure of some circuit in the broadband power analog signal path (see Figure 8-F-1).

6. Failure of the Underload/Overload Detector circuit on A4.

7. Incorrect trip point settings for the Underload/Overload Detector.

8-F-13. Problems 1, 2, and 3 in paragraph 8-F-12 can usually be seen by selecting ENTRY 100 and WIDEBAND mode. If the observed signal in the MEASUREMENT/ENTRY display is "racking" continuously when it should represent a stable, pure, broadband power input signal, the problem should be either a failure of A2 or A4, or a bad input signal. Try another signal source first to eliminate that possibility. Problem 4 can be verified by forcing a CAL cycle to occur. If a CAL error code of the form CE-N (where N = 0-9, A, or b) oc-

curs, one or more of the RF Gain steps is not being selected correctly. This could be caused by a bad relay driver or a faulty relay on A2. Problem 5 requires standard signal tracing using Figure 8-F-4.

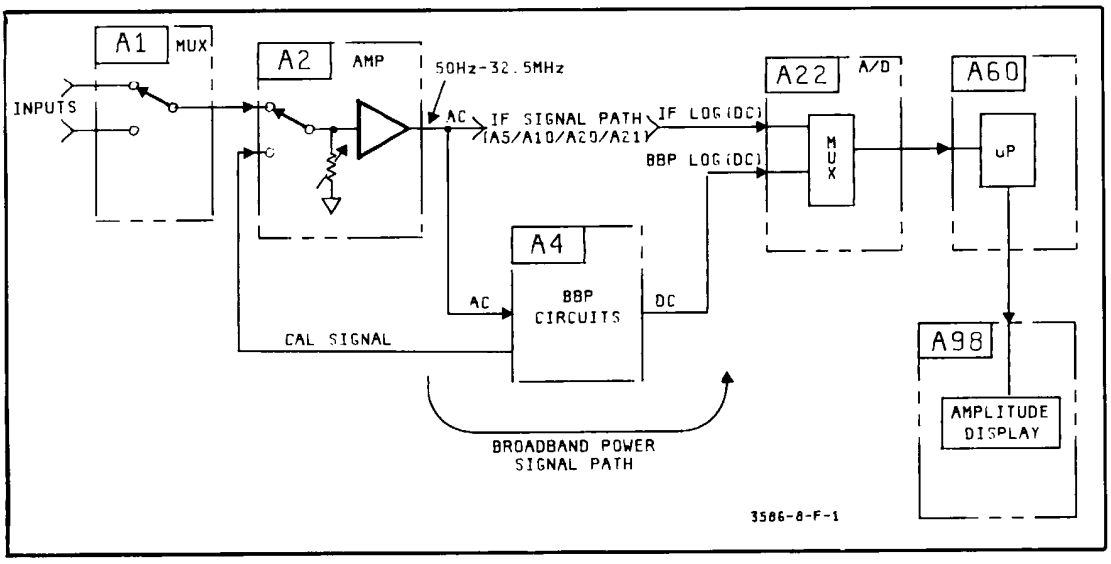


Figure 8-F-1. Broadband Power (BBP) Signal Path.

8-F-14. Problems 6 and 7 are tied together. Use Tables 8-F-1 and 8-F-2 to see if the trip points are being set correctly. Note that the voltage at TP8 should always remain constant for a Full-Scale input signal regardless of the selected mode or Full Scale setting. The different trip point settings compensate for the differing input signal levels to the Detector/Logger circuit as shown by the tables. By holding the Full Scale setting constant and by raising or lowering the level of the input signal above or below Full Scale, the actual input voltages to the Underload/Overload Detector can be monitored. It is then relatively easy to verify that the detector is working by watching the red and yellow LED's on A4, and/or monitoring the status (HIGH or LOW) of the UNDERLOAD/OVERLOAD lines to A60. Refer to the schematic (Figure 8-F-2). For example, if the input signal level is greater than the Full Scale setting, the voltage at TP8 will be less than +5.0 Volts. If the voltage drops below about +4.85V (equivalent to about +1.0dB above Full Scale), comparator U6B should trip, U6(7) should go to the positive rail and XA4 (B14) should go HIGH (about +1.8V) signaling an OVERLOAD condition to the A60 processor. If the signal level drops below full scale, when the voltage at TP8 exceeds +6.65V (about −7.5dB below Full Scale), comparator U6A should trip and XA4 (A14) should go HIGH signaling an UNDERLOAD condition to the processor.

Table 8-F-1. Underload/Overload Trip Point Settings.

Mode	Full Scale Setting	(Δ5dB) Thresh 1	(Δ10dB) Thresh 2	Full Scale Voltage TP7	Full Scale Voltage TP8	Trip Points
LO NOISE (LN)	−30dBm	H	H	−.25V	+5.0V	0dB
LO DIST (LD)	−30dBm	L	H	−.30V	+5.0V	−5dB
(LN) and (LD)	−40dBm	H	L	−.35V	+5.0V	−10dB
(LN) and (LD)	−45dBm	L	L	−.40V	+5.0V	−15dB
WIDEBAND	−30dBm	L	H	−.30V	+5.0V	−5dB

NOTES:
1. Voltages are ±10%.
2. H = +3.8V, L = +.26V at XA4 (A13, B11).
3. ENTRY 100, Full Scale input signal at the tuned frequency.
4. See also Table 8-F-2 (Trip Point Thresholds vs. Full Scale Settings).

Table 8-F-2. Trip Point Thresholds vs. Full Scale Settings.

	LO DIST		LO NOISE		WIDEBAND	
Full Scale	TH 1	TH 2	TH 1	TH 2	TH 1	TH 2
+25	H	H	H	H	--	--
+20	L	H	H	H	L	H
↕	↕	↕	↕	↕	↕	↕
-30	L	H	H	H	L	H
-35	L	H	L	H	L	H
-40	H	L	H	L	--	--
-45	L	L	L	L	--	--

NOTES: 1. ENTRY 100 used to select Full Scale setting.
2. H = +3.8V, L = +.26V at XA4 (A13, B11).
3. See also Table 8-F-1 (Underload/Overload Trip Point Settings).

8-F-15. It should be noted that some operational usages of the 3586 require that an input signal have amplitude modulation present. If continuous autoranging occurs in these situations, especially when low frequencies (<100Hz) or low signal levels are involved, selecting AVEraging to ON will often cure the problem. If not, the ENTRY mode of setting Full Scale should be used. See also "Auto-Range Problems" in Table 8-9.

8-F-16. Broadband Power (WIDEBAND) Problems.

8-F-17. If a discrete frequency input signal of known amplitude is applied to the input and its amplitude is correctly measured by the 3586 in LO DIST, but a large amplitude error exists in WIDEBAND, the problem could be due to one of the following causes:

1. A2 output buffer failure (BBP signal path).
2. A4 BBP signal path circuit failure.
3. A22 input buffer or input multiplexer failure.

8-F-18. Problems 1 and 2 in paragraph 8-F-17 can be checked by signal tracing using Figure 8-F-4. Problem 3 can be checked by monitoring the voltage at A4TP7 while varying the amplitude of the input signal. In LO DIST mode, a Full Scale signal should read −.3VDC and should change by 10 millivolts/dB as the input signal is reduced below Full Scale until, at 80dB below Full Scale, TP7 should read about −1.1VDC. If this check proves correct, the problem is most likely at the input circuits on A22.

8-F-19. Underload/Overload Problems.

8-F-20. Some underload/overload condition indications are normal operation for the 3586. For example, if the manual ENTRY method of setting Full Scale has been selected by the operator, and he then inputs a signal that is too far above or below the current Full Scale setting, an overload/underload condition does exist and should be so indicated on the front Panel. See the discussion under "Overload/Underload Indications" in Table 8-9 for more detailed information.

8-F-21. For those situations which are not normal, the Underload/Overload Detector circuits can be checked using the procedure described in paragraph 8-F-14.

8-F-22. Calibration Problems.

8-F-23. A detailed discussion on troubleshooting calibration problems may be found under "Calibration Problems" in Table 8-9. Other information on the CAL cycle is contained in paragraphs 8-30 and 8-32. See also Table 8-F-3 and the information in paragraphs 8-F-24 to 8-F-26.

Table 8-F-3. Calibration Error Codes.

Format is CE-N Where N =	Item Under CAL	Suspect Cards
Ø to 9, A, b	RF Gain, Step N	A2*
C	400Hz Filter	A10, A20
d	20Hz Fillter	A20
E	10/100dB or WIDEBAND	A21, (A4)**
F	Weighted Filter	A21, A22, A70***

* If *all* RF Gain steps fail, the problem could be anywhere in the receiver circuits. Press MEAS CONT to exit the CAL cycle and run TF 13 (paragraph 8-81).

** If CAL is performed in WIDEBAND, the A4 BBP circuits are calibrated instead of the IF signal path through A21.

*** If A60S2(2) is OPEN and an A70 Impairments board (Option 003) is not installed, CE-F will *always* occur during the CAL cycle.

8-F-24. When the CAL cycle is performed in WIDEBAND, the First L.O. frequency is automatically set to 51.23MHz by the processor so that the A15 tracking output (and therefore the calibration signal frequency) will be 1.23MHz. After the CAL cycle is finished, the First L.O. frequency is restored to whatever it was before the CAL cycle began.

8-F-25. When the CAL cycle is performed in LO DIST or LO NOISE, the First L.O. is automatically set to a frequency 50Hz lower than it was, for the duration of the CAL cycle. This is to allow an accurate CAL constant to be derived, free from the influence of any very strong input signal simultaneously present within the instrument (on A1). Also, if the 3586 is tuned to a frequency below 20kHz when a CAL cycle is performed, the First L.O. is automatically set to 50.020MHz for the duration of the CAL cycle so that the CAL signal frequency is 20kHz. If AVE is on when CAL occurs, it is turned off for the duration of CAL and then turned back on.

8-F-26. If CAL is not working at all but the 3586 appears to measure input signals correctly, the CAL signal may not be getting turned on. The (L) CAL command signal from the processor that should turn on the CAL signal goes two places. On A15, it turns off A15Q4 which allows the tracking output signal to be sent to A4 for use as the CAL signal. On A4, it turns off A4Q101 which allows A4 to accept the tracking output signal. If either A15Q4 or A4Q101 were shorted, CAL could not turn on.

8-F-27. A4 Troubleshooting Hints.

8-F-28. When checking the 80Hz Oscillator and the Sampling VCO, one end of R1 (ØΩ) may be lifted to obtain a stable sampling VCO frequency. The 80Hz Oscillator normally frequency modulates the Sampling VCO output between 20kHz and 50kHz so with R1 lifted it should oscillate somewhere in that frequency range. Also, if the 80Hz Oscillator is running

low in frequency (e.g. 60Hz), it can beat with the power line frequency causing auto-range problems. A possible auto-range problem on earlier serial number instruments might be cured by the newer component values for A4R43 and A4R45. Old values (Serials prior to 1927A-00101) were 46.4kΩ (A4R43) and 52.3kΩ (A4R45). Newer instruments may have either 53.6kΩ or 56.2kΩ for A4R43 and 56.2kΩ or 61.9kΩ or A4R45.

8-F-29. If the Calibration signal flatness needs adjusting, always adjust L106 *before* C113. If BBP linearity problems exist, check the Sampler circuit diodes first since the range of the Detector/Logger is more than adequate to handle frequency response. To check the Detector/Logger, lift one end of C26 and inject an A.C. signal at TP5 while measuring the D.C. output voltage of U4 at TP7. The Detector Logger should respond linearly according to Table 8-F-4. To check the Detector/Logger using an input signal, leave C26 in the circuit, select ENTRY 100, set Full Scale to ØdBm and input signals as shown in Table 8-F-4.

Table 8-F-4. Detector/Logger Linearity.

Input Signal Relative To Full Scale		Volts (pk-pk) TP5		Volts D.C. U4(6)		Volts D.C. TP7	
A	B	A	B	A	B	A	B
+5dBm	+5dBm	6.0 V	6.0 V	+45mV	+45mV	-.25V	-.25V
ØdBm	--	3.5 V	--	+62mV	--	-.30V	--
--	-1dBm	--	3.0 V	--	+65mV	--	-.31V
-5dBm	--	1.9 V	--	+79mV	--	-.35V	--
--	-7dBm	--	1.5 V	--	+85mV	--	-.37V
-10dBm	--	1.1 V	--	+95mV	--	-.40V	--
--	-13dBm	--	.75V	--	-105mV	--	-.43V
-15dBm	--	.60V	--	+112mV	--	-.45V	--
--	-19dBm	--	.38V	--	+125mV	--	-.49V
-20dBm	--	.35V	--	+128mV	--	-.50V	--
-25dBm	-25dBm	.19V	.19V	+145mV	+145mV	-.55V	-.55V
-30dBm	--	.14V	--	+161mV	--	-.60V	--
--	-31dBm	--	.10V	--	+165mV	--	-.61V

NOTES: 1. (A) readings are for 5dB steps of the input signal.
2. (B) readings are for 6dB steps of the input signal.
3. Voltages are calculated values and may actually be ±10%.

8-F-30. Tracking Output (A15) Troubleshooting.

8-F-31. Troubleshooting A15 should be a fairly straightforward operation using Figure 8-F-4. Verify the two input signals (50MHz from A40 and First L.O. from A51) are present first, then check that the mixer output frequency as seen at TP1 and TP3 is equal to the difference of the two mixer input frequencies. If the frequencies are correct but the levels are not close to the values indicated on the functional block diagram, suspect the leveling loop.

8-F-32. The tracking output signal (0-32.5MHz) at A15J2 is meant to be used by external instruments for tracking the 3586 tuned frequency. The level of this signal is normally verified to be 0 ± .2dBm at 10kHz. All other 5MHz points (from 0-30MHz) are then checked to be within ± .25dB of the actual level noted at 10kHz. To maintain this output level close to ØdBm at all frequencies from 0 - 32.5MHz, a leveling feedback loop is used. The output signal is tapped at TP2 and its level measured by a Peak-to-Peak detector.

8-F-33. If the tracking output signal is not ØdBm ± 0.5dB from 0 - 32.5MHz, the leveling loop may be at fault. The voltages in the Peak-to-Peak detector circuit are critical for correct leveling to occur. If the loop is suspected, lift the end of R8 which connects to TP6 and connect a DC source to R8. If a DC voltage from 0 to +1V is applied to R8, it should change

the level of the 50MHz input to U1 by changing the operating impedance of CR2 (as the leveling loop is *supposed* to do). This in turn should vary the mixer output level and thus the tracking output level. If it does, suspect U3 or CR3 - CR7. If it does not affect the mixer output level, suspect mixer U1 and CR2. It is also possible for U2 to affect the tracking output flatness.

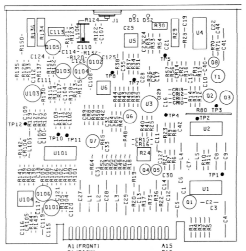
8-F-34. The CAL output portion of A15 is easily verified. A signal should not be present at TP4 unless the CAL cycle (about 3 seconds maximum), TF2 (paragraph 8-58), or TF12 (paragraph 8-79) are active. When CAL or TF2 are active, TP4 will have a 1MHz signal present. Only one signal (or neither) should be present at the input to U5D at one time, never both. The signals at U4 and U5 are all ECL levels (+4.1VDC peak to +3.2VDC base). At TP4, the signals are 160mVp-p (from +1.2VDC peak to +1.04VDC base) due to the action of R47 and R48 as a voltage divider.

8-F-35. In LO DIST and LO NOISE modes, any difference in frequency between the tracking output and the front panel tuned frequency indicates a problem. If the First L.O. frequency at A15J1 is equal to the front panel tuned frequency +50MHz, then the First L.O. is correct and the problem is probably the Mixer A15U1. If not, then the problem is somewhere in the First L.O. boards. Refer to Service Group D for procedures to troubleshoot the First L.O. signal. The tracking output may *normally* disagree with the front panel when the selected mode is *not* LO DIST or LO NOISE. See Table 8-F-5 for normal tracking output frequencies versus mode selections.

Table 8-F-5. Tracking Output Frequencies vs. Mode Selections.

Measurement Mode Selection	Entry Frequency	Channel	Tracking Output Frequency #
LO DIST, LO NOISE, WIDEBAND	*	*	1,000,000Hz
NOISE/DEMOD, NOISE/TONE, PHASE JITTER, IMPULSE	CARRIER	↗	1,001,850Hz
	CARRIER	↘	998,150Hz
	TONE	↘	999,154Hz (998,950Hz)
	TONE	↗	1,000,846Hz (1,001,050Hz)
TONE 1004Hz (TONE 800Hz) #	TONE	*	1,000,000Hz
	CARRIER	↘	998,996Hz (999,200Hz)
	CARRIER	↗	1,001,004Hz (1,000,800Hz)
CARRIER	CARRIER	*	1,000,000Hz
	TONE	↘	1,001,004Hz (1,000,800Hz)
	TONE	↗	998,996Hz (999,200Hz)
SIGNAL 2600Hz (1010Hz) #	TONE	↗	1,001,596Hz (1,000,210Hz)
	TONE	↘	998,404Hz (999,790Hz)
	CARRIER	↘	997,400Hz (998,990Hz)
	CARRIER	↗	1,002,600Hz (1,001,010Hz)

NOTES: 1. All readings taken with front panel tuned frequency = 1,000,000Hz.
2. # Where only one frequency is given, applies to 3586A/B. Where two frequencies given, first = 3586B, second ( ) = 3586A.
3. * Selection has no effect on T. O. frequency.



A4
-bp- Part No. 03586-66504
Rev C

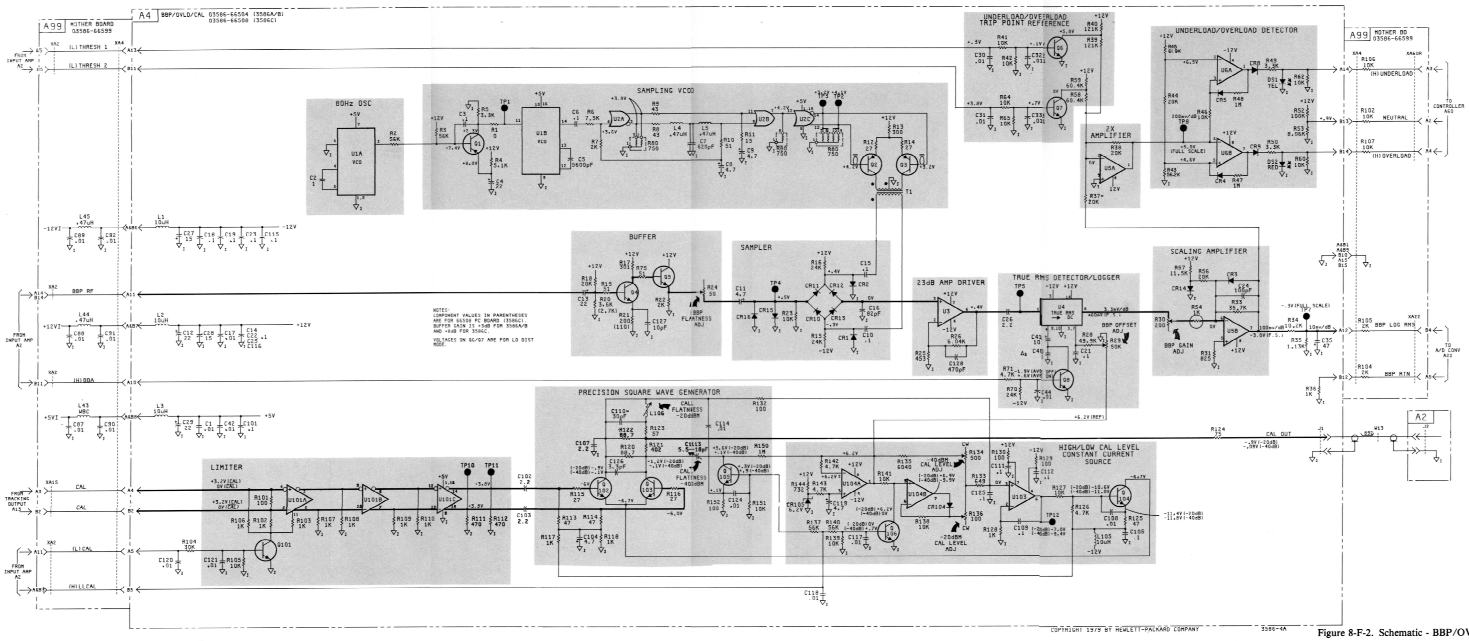
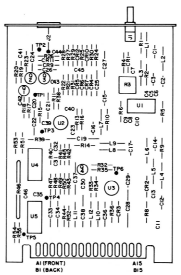


Figure 8-F-2. Schematic - BBP/OVLD/CAL (A4)



A15
hp Part No. 03586-66515
Rev A
3586-15C

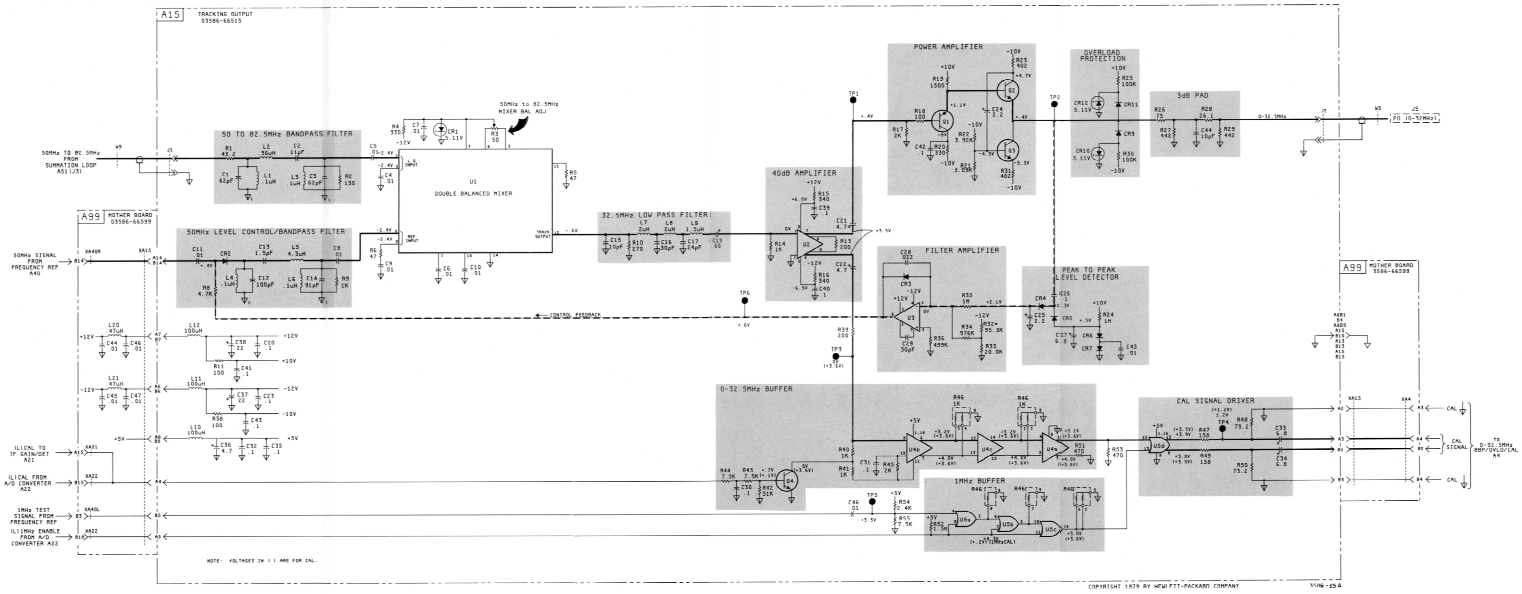


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Figure 8-F-3. Schematic - Tracking Output (A15)
8-F-11/8-F-12

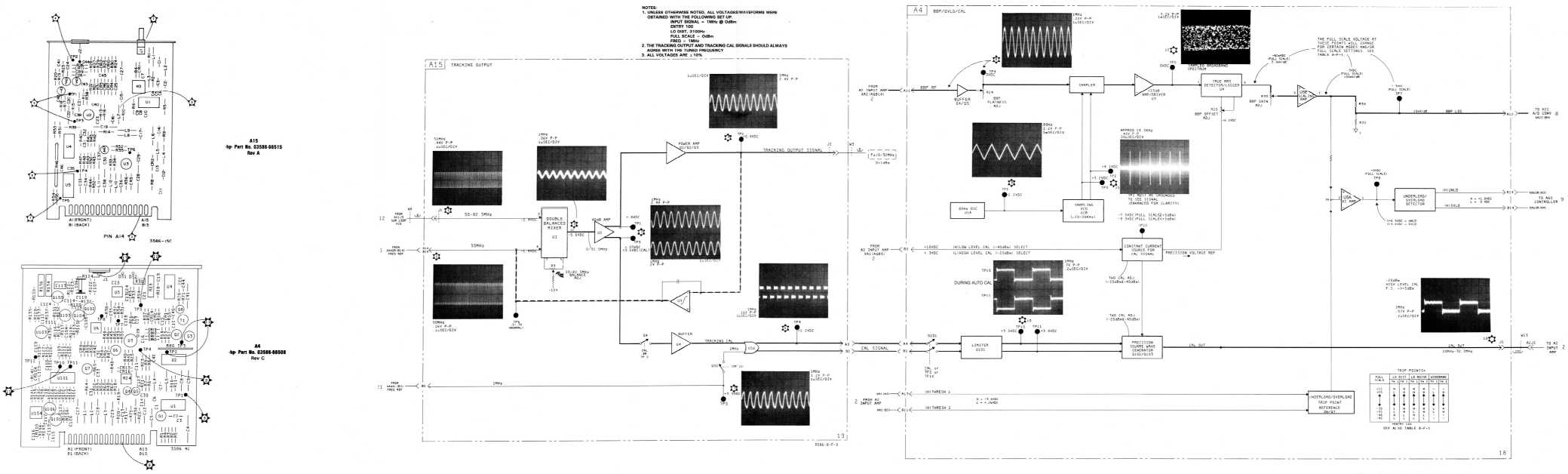

Figure 8-F-4. Functional Block - CAL/BBP/TRACK (A4/A15)
8-F-13/8-F-14

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IMPAIRMENTS
SERVICE GROUP G

Contents

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8-G-1. ADJUSTMENTS (CROSS REFERENCE).

8-G-2. Phase Jitter Adjustments.

Designation	Adjustment Title	Paragraph
A70R181	VFD FREQ ADJ	5-22
A70R146	PHASE JITTER GAIN ADJ	5-22
A70R133	PHASE JITTER 20Hz ADJ	5-22
A70R125	PHASE JITTER 4Hz ADJ	5-22

8-G-3. Notch Filter Adjustments.

Designation	Adjustment Title	Paragraph
A70R33	NOTCH 2	5-22
A70R40	NOTCH 1	5-22
A70R45	NOTCH 3	5-22

8-G-4. Logger Adjustments.

Designation	Adjustment Title	Paragraph
A70R70	LOGGER OFFSET ADJ	5-22
A70R72	LOGGER GAIN ADJ	5-22

8-G-5. Impulse Noise Adjustments.

Designation	Adjustment Title	Paragraph
A70R102	COMPARATOR REF ADJ	5-22
A70R97	DEAD TIMER ADJ	5-22

8-G-6. THEORY OF OPERATION (CROSS REFERENCE).

8-G-7. Phase Jitter - Paragraph 8-276.

8-G-8. Weighted Filter/Notch Filter - Paragraph 8-281.

8-G-9. Impulse Noise Circuits - Paragraph 8-285.

8-G-10. Calibration Oscillator - Paragraph 8-288.

8-G-11. TROUBLESHOOTING DATA.

8-G-12. General Information.

8-G-13. The A70 performs all of its functions (Phase Jitter measurements, Weighted/Notch Filter operation, Impulse measurements) on the SSB Demodulated audio from the A21 board. To check A70 operation, therefore, verify that a good, clean audio signal is available at the input (A70TP8) and trace it through the appropriate circuits.

8-G-14. To get a 1850Hz full-scale signal at TP8, perform the following steps:

1. On the 3586A/B, press RECALL, Ø to restore turn-on conditions.

2. Select ENTRY 100 and set Full Scale to ØdBm.

3. Input 1MHz at ØdBm. Be sure the selected termination impedance matches the signal source.

4. TP8 should now have a 1850Hz signal at 2.2Vp-p as seen on an oscilloscope or 0.75 VRMS as measured on a DVM.

8-G-15. Another method of obtaining an audio signal of the desired frequency and amplitude at A70TP8 is to disconnect all external signals, press RECALL, Ø to restore turn-on conditions, activate TF12 (paragraph 8-79), and then select ENTRY 100 and a full scale setting of −40dBm. This will give you a full scale signal in to A70TP8 of 2.2Vp-p at 1850Hz. If you now selectively change the front panel turned frequency of the 3586 by a given amount (e.g., 100Hz), the signal frequency at A70TP8 will change by the same amount. Within the range of the selected bandwidth, the amplitude of the signal should stay about the same at TP8 or about 2.2Vp-p.

8-G-16. Phase Jitter Troubleshooting.

8-G-17. To measure residual phase jitter, follow steps 1-3 in paragraph 8-G-14 (except input a 1.001MHz signal at ØdBm) and then select ϕ JITTER mode. TP8 should now have a clean 1000Hz sine wave at 2.2Vp-p. The residual phase jitter displayed on the front panel should be less than 0.5°p-p. If it is greater than 0.5°, check the waveforms at TP8, TP9, TP10, and TP11 as shown on Figure 8-G-4. If they are good, check U29(3) for Ø VRMS. If U29(3) is good, check U30(1) for Ø VDC. If U30(1) is good, the problem may be noise on the A/D board. Go to Service Group C and check all the inputs to the A/D for noise. If the signal at TP8, TP9, TP10, TP11, U29(3) or U30(1) is bad, suspect the preceding stage. If there is any doubt as to how "clean" the input signal at TP8 is when a high residual phase jitter is present, look at the signal with a spectrum analyzer for the presence of sidebands.

8-G-18. If residual phase jitter is acceptable, the following procedure will verify phase jitter operation.

1. Set up two sources with the same output impedance (e.g. 75 ohms) with one at 1.001MHz/ØdBm and the other at 1.001150MHz/ −20dBm.

2. Connect the two sources to the same input termination impedance (e.g., 75 ohms) on the 3586 using a power combiner (see Table 8-14, "Recommended Test Equipment").

3. Press RECALL, Ø to restore turn-on conditions.

4. Turn on counter. Display should read 1.001MHz at approximately −6dBm.

5. Select ϕ JITTER mode.

6. Display should read +11.5° (±0.1°) p-p. If it does not, check the waveforms at TP8, TP9, and TP11. They should be as shown on Figure 8-G-4 except for some jitter (150Hz) on the rising and falling edges. There should be no jitter on the waveform at TP10, otherwise it should look the same as that on TP9 and should always track TP9 exactly in frequency.

7. If these points are good, check U29(3) for a 150Hz sine wave at 3.8v(p-p). The same signal should be at the ϕ JITTER AC out BNC on the rear panel. If these are good, check U30(1) for −1.9vdc (= +11.5°p-p). If good, problem is on the A/D board (A22). If bad, problem is in the Peak-to-Peak Detector circuit. Note that the $\frac{\text{p-p}}{2}$ value of the ϕ JITTER AC out should equal the ϕ JITTER DC output value.

8-G-19. Phase Jitter Error Codes.

8-G-20. Error Code E 2.2 indicates that the input signal to the 3586 is 40dB or more below the current Full Scale setting and is not of sufficient level to accurately make a phase jitter measurement. This is determined by the processor taking an IF amplitude measurement from A21 and therefore has nothing to do with the status of the A70 board.

8-G-21. Error Code E 2.3 is an indication that the tone frequency upon which phase jitter measurements are being attempted is not within 960-1060Hz and therefore is not valid. If the tone is known to be within this range, A70R181 may need adjusting. This pot moves a 100Hz "window" all at once. For example, if the present limits for a valid signal were 900-1000Hz, adjusting A70R181 could move the window back to 960-1060Hz where it belongs. When the tone is valid, the voltage at U26(6/10) will be between that at U26(2) and U26(11). U26(4) will be LOW, U26(5) will be HIGH and U26(2) will be HIGH (valid). If the tone exceeds 1060Hz, the voltage at U26b(6) will be greater than 4.6V. This in turn, will cause U26b(1) to be LOW along with U26a(5). U26a(2) will also go LOW. If the tone goes less than 960Hz, the voltage at U26d(10) will be less than 3.5V. This causes U26(13) to go HIGH in conjunction with U26a(4). The "greater" amplitude at the negative input of U26a will cause U26a(2) to go LOW, again indicating an invalid signal. (See Section VII (Δ11).)

8-G-22. Error Code E 2.9 indicates that the phase jitter DC output to the A22 A/D Converter is not between Ø and −2.0 vdc as measured at the A/D. There is a voltage divider on A22 that reduces the output of A70U30(1) to an acceptable level for the A/D with a maximum of −2.0 vdc being equivalent to about 40°p-p of phase jitter. The A70 board is capable of measuring larger levels of phase jitter but a practical level of information is quickly exceeded past 40°p-p. Since the scale factor for the output at U30(1) is 6°/−1 vdc,

the −6.67 dc at U30(1) is equivalent to 40°p-p of phase jitter. The voltage divider inputs 30% of this to the A/D (or −2.0 vdc) and if this level is exceeded, E 2.9 is displayed. A70R146 adjusts the gain of U28A so that 6° of phase jitter is equal to −1.0 vdc.

8-G-23. Weighted Filter Troubleshooting.

8-G-24. To check the Weighted Filter, use the following procedure.

1. Perform all the steps in paragraph 8-G-14.

2. Connect a scope to TP1.

3. With 3100Hz bandwidth selected, TP1 should have the 1850Hz waveform shown there in Figure 8-G-4 with a p-p value of 4.5v which is double (or +6dB) that at TP8 (2.2v p-p Full Scale).

4. Select WTD 3100Hz bandwidth.

5. The signal level at TP1 should drop about 15% as the weighted filter is switched in. Example: 4.5v (p-p) to 3.7v (p-p). This is true only for a signal with a frequency of 1850Hz. Other frequencies will yield different results.

8-G-25. For a 3586B, a 1000Hz signal at TP1 will stay the same amplitude with the weighted filter in. For a 3586A, 800Hz at TP1 will stay about the same amplitude with weighting. Frequencies other than 800Hz or 1000Hz should get some level reduction at TP1 when the weighted filter is switched in (depending on the frequency). To vary the frequency at TP1 (and TP8), simply vary the input signal frequency or the 3586 tuned frequency as necessary to obtain the desired frequency. When the tuned and input frequencies are the same, TP1 and TP8 will have 1850Hz present in LO DISTortion mode. See Table 8-G-1 for some typical amplitude reductions (for comparison only) at different frequencies for a 3586B "C-Message" weighted filter. A 3586A "Psophometric" weighted filter would have similar values. Note that if a full-scale input signal to the 3586 does not produce a full scale audio signal (2.2Vp-p or 0.75 VRMS) at TP8, the problem is most likely **not** on A70. (See Service Group B for troubleshooting audio problems.)

Table 8-G-1. C-Message Filter Weighting.

Input Frequency (A70TP8)	Weighted Signal Amplitude (A70TP1)	Signal Reduction In dB Relative to 1KHz
400Hz	1.2V (p-p)	−12.2dB
500Hz	1.8V (p-p)	− 7.7dB
600Hz	2.5V (p-p)	− 4.6dB
700Hz	3.2V (p-p)	− 2.5dB
800Hz	3.8V (p-p)	− 1.1dB
900Hz	4.2V (p-p)	− 0.3dB
1000Hz	4.3V (p-p)	0
1200Hz	4.2V (p-p)	− 0.2dB
1400Hz	4.0V (p-p)	− 0.7dB
1600Hz	3.8V (p-p)	− 1.1dB
1850Hz	3.7V (p-p)	− 1.3dB
2000Hz	3.7V (p-p)	− 1.3dB
2500Hz	3.6V (p-p)	− 1.6dB
3000Hz	3.2V (p-p)	− 2.8dB
3100Hz	2.9V (p-p)	− 3.4dB
3200Hz	2.7V (p-p)	− 4.3dB
3300Hz	2.5V (p-p)	− 5.3dB

8-G-26. Notch Filter Troubleshooting.

8-G-27. To check the 1010Hz notch filter, use the following procedure.

1. Perform steps 1-3 in paragraph 8-G-14 except input 1001500Hz at ØdBm.

2. Select NOISE/TONE mode on the 3586.

3. A70TP8 should now have a 1500Hz full-scale signal at 2.2Vp-p on a scope.

4. A70TP1 should have the same 1500Hz at about 4.4Vp-p.

5. A70TP2 should have the same 1500Hz at about 10.8Vp-p. Leave the oscilloscope on TP2.

6. Step (or sweep) the input source from 1001500Hz down to 1000500Hz in 10Hz increments while observing the signal at TP2.

7. The signal should decrease in amplitude as the frequency approaches the center of the notch until, at notch center (1010Hz), there is only noise present (usually <20mVp-p). As the input signal leaves 1001010Hz and approaches 1000500Hz, the signal should again increase in amplitude until it is about 10Vp-p at 1000500Hz.

8-G-28. Table 8-G-2 gives some typical amplitude values (for comparision only) of frequencies close to the notch. Sample checks from Table 8-G-2 should help to identify problem areas in the notch filter.

Table 8-G-2. Notch Filter-Frequency Versus Amplitude.

Input Frequency (A70TP8)	Signal Amplitude (A70TP2)	Signal Reduction In dB Relative to 2KHz
1200Hz	9.2V (p-p)	- 1dB
1150Hz	5.3V (p-p)	- 6dB
1100Hz	1.4V (p-p)	- 17dB
1090Hz	1.0V (p-p)	- 20dB
1080Hz	0.65V (p-p)	- 24dB
1070Hz	0.42V (p-p)	- 28dB
1060Hz	0.24V (p-p)	- 32dB
1050Hz	0.12V (p-p)	- 39dB
1040Hz	50mV (p-p)	- 46dB
1030Hz	20mV (p-p)	- 59dB
1020Hz	10mV (p-p)	- 78dB
1010Hz (NOTCH)	10mV (NOISE)	- 81dB (NOTCH)
1000Hz	10mV (p-p)	- 78dB
990Hz	20mV (p-p)	- 61dB
980Hz	50mV (p-p)	- 48dB
970Hz	0.12V (p-p)	- 40dB
960Hz	0.27V (p-p)	- 34dB
950Hz	0.43V (p-p)	- 27dB
940Hz	0.72V (p-p)	- 23dB
930Hz	1.1V (p-p)	- 19dB
920Hz	1.7V (p-p)	- 16dB
910Hz	2.5V (p-p)	- 12dB
900Hz	3.5V (p-p)	- 9dB
850Hz	9.0V (p-p)	- 1dB
800Hz	10.1V (p-p)	ØdB

8-G-29. Audio Detector/Logger Troubleshooting.

8-G-30. If the Detector/Logger (A70U22) is suspected to be bad, **first** swap the IC (U22) with the same IC on the A4 board (A4U4). Both of these chips are in sockets for this very purpose as is also the same IC on the A21 board (A21U5). All three chips have the same part number and are completely interchangeable although some gain/offset readjustments may be required after permanent replacement.

8-G-31. If no changes in problem symptoms occur after swapping A70U22 with A4U4, replace the chips in their original positions to eliminate circuit readjustments. However, if WIDEBAND amplitude errors occur with these two chips swapped, or front end overload/underload problems or auto-ranging problems now exist, the A70U22 chip was bad and should be replaced.

8-G-32. One way to check the logger circuits for other problems is to input a full scale signal to the A70 board and trace it through the Logger Range Expander and Detector/Logger circuits. Use the following procedure.

1. Perform steps 1-4 in paragraph 8-G-14.

2. A70TP1 should have a 1850Hz signal at about 4.4Vp-p and A70TP2 should have the same signal at about 10.8Vp-p. A70TP6 should have about +0.052 VDC and U10(1) should have about −0.3 VDC. All of these values represent a full-scale signal into A70 at TP8 and may be used to locate the general area of a discrepancy.

8-G-33. If the problem is one of logger accuracy versus input signal amplitude, use Table 8-G-3 to verify circuit operation for input signal levels that are below the Full Scale setting. The table is for comparison purposes only.

Table 8-G-3. A70 Signal Voltages Versus Input Signal Level.

Input Relative To Full Scale	TP8	TP1	TP2	TP7	TP6	U10(1)
ØdB	2.2V (p-p)	4.4V (p-p)	10.8V (p-p)	7.8V (p-p)	+0.052 VDC	−0.30 VDC
− 5	1.2V	2.5V	6.0V	5.8V	+0.060	−0.35
−10	0.68V	1.4V	3.4V	4.4V	+0.068	−0.40
−15	0.38V	0.8V	1.9V	3.4V	+0.076	−0.45
−20	0.22V	0.45V	1.1V	2.5V	+0.084	−0.50
−25	0.12V	0.25V	0.6V	1.9V	+0.092	−0.55
−30	70Mv	0.14V	0.34V	1.4V	+0.100	−0.60
−35	40mV	80mV	0.19V	1.0V	+0.108	−0.65
−40	25mV	45mV	0.11V	0.8V	+0.116	−0.70
−45	15mV	26mV	60mV	0.6V	+0.124	−0.75
−50	10mv	16mV	40mV	0.45V	+0.132	−0.80
−55	7mV	11mV	20mV	0.35V	+0.140	−0.85
−60	5mV	6mV	15mV	0.25V	+0.148	−0.90
−65	5mV	5mV	10mV	0.20V	+0.156	−0.95
−70	5mV	5mV	8mV	0.15V	+0.164	−1.00
−75	5mV	5mV	5mV	0.13V	+0.172	−1.05
−80dB	5mV (p-p)	5mV (p-p)	5mV (p-p)	0.10V (p-p)	+0.180 VDC	−1.10 VDC

Notes:

1. Signal frequency used for above measurements was 1850Hz at A70TP8 as set up by paragraph 8-G-14.
2. Voltages are for comparison purposes only.
3. Typical voltage gain of U10A as set by R72 is approximately −6.
4. Note that U10(1) changes .05 VDC for each 5dB change in input signal.

8-G-34. Impulse Noise Circuit Troubleshooting.

8-G-35. To check the Impulse circuits up to the Comparator (U19) inputs, use the following procedure.

1. Perform steps 1-4 of paragraph 8-G-14.

2. TP2 should have a 1850Hz signal at about 10.8Vp-p.

3. TP4 should have the same signal rectified or about 5.4V (peak) and double the number of positive peaks (3700Hz).

4. TP5 should have +5.9V for a 3586A or B.

5. Select IMPULSE mode and press START.

6. TP5 should read about +3.65 vdc (THRESHOLD should still be ØdBm and Full Scale should be ØdBm from step 1 above).

7. Select other values of THRESHOLD settings from Table 8-G-4 and check TP5 for the approximate voltage indicated. Note that the voltage difference from instrument to instrument for any one frequency and full scale setting may cover ±3dB of CAL error. The CAL constant is **always** added to the value supplied to the D/A Converter as a reference for the Comparator (U19) and it cannot be zeroed out. However, the relative readings for sequential threshold steps within one instrument should remain about the same for a given frequency and full scale setting. Table 8-G-4 gives typical values for comparison purposes **only**. If the values for TP6 change with threshold changes and correspond approximately with Table 8-G-4, it shows that U14-U18 and U41 are probably all working.

8-G-36. To check the Comparator (U19) use the following procedure.

1.Perform steps 1-3 of paragraph 8-G-14 except set the input signal frequency to 1,000,500Hz at ØdBm. This will place a 500Hz full scale signal at TP2 which will not be affected by the Notch filter when IMPULSE mode is selected. Threshold will automatically be set equal to ØdBm.

2. Select IMPULSE but do not press START yet.

3. TP4 should have a rectified 500Hz signal with peak values of about +5V.

4. Look at U19(7) with a scope. It should hve a constant DC output of about +0.1V.

Table 8-G-4. Impulse Threshold D/A Conversions.

	A70TP5	
THRESHOLD (T) Settings	**3586B**	**3586A**
0/-15/-30/-45dBm	+3.651 VDC	+5.089 VDC
-1/-16/-31/-46dBm	+3.259 VDC	+4.555 VDC
-2/-17/-32/-47dBm	+2.906 VDC	+4.064 VDC
-3/-18/-33/-48dBm	+2.591 VDC	+3.625 VDC
-4/-19/-34/-49dBm	+2.296 VDC	+3.232 VDC
-5/-20/-35/-50dBm	+2.042 VDC	+2.865 VDC
-6/-21/-36/-51dBm	+1.825 VDC	+2.547 VDC
-7/-22/-37/-52dBm	+1.625 VDC	+2.277 VDC
-8/-23/-38/-53dBm	+1.450 VDC	+2.027 VDC
-9/-24/-39/-54dBm	+1.292 VDC	+1.809 VDC
-10/-25/-40/-55dBm	+1.159 VDC	+1.612 VDC
-11/-26/-41/-56dBm	+1.024 VDC	+1.446 VDC
-12/-27/-42dBm	+0.924 VDC	+1.278 VDC
-13/-28/-43/+2dBm	+4.590 VDC	+1.154 VDC
-14/-29/-44/+1dBm	+4.079 VDC	+5.727 VDC
+3dBm	+5.000 VDC	+6.250 VDC
T > +3dBm	E6.2**	E6.2**
T < -56dBm	E6.1***	E6.1***

Notes:

1. All readings were taken with Full Scale setting = ØdBm (ENTRY 100) and 3586 frequency = 1MHz. For other frequencies and/or other full scale settings, equivalent readings (±25%) will occur anytime the threshold setting is the same number of dB below the Full Scale setting. Readings are for comparison only.

2. START must be pressed to see the new value at TP5 after the Threshold setting is changed.

3. When T = +3dBm to -12dBm, U16 (12,15,19) = 110, for U39 A gain = ØdBm and U39B = ØdBm.

When T = -13dBm to -27dBm, U16 (12,15,19) = 010, for U39A gain = 15dBm and U39B = ØdBm.

When T = -28dBm to -42dBm, U16 (12,15,19) = 101, for U39A gain = ØdBm and U39B = 30dBm.

When T = -43dBm to -56dBm, U16 (12,15,19) = 011, for U39A gain = 15dBm and U39B = 30dBm.

4. *All codes are TTL, where 0 = +0.2 VDC and 1 = +4.5 VDC.

**A70TP5 has last valid reading still present. See paragraph 8-G-41 for E6.2 discussion.

***A70TP5 has last valid reading still present. See paragraph 8-G-40 for E6.1 discussion.

5. For additional information, see paragraph 8-G-35.

5. Press START. U19(7) should now have a 1KHz square wave output at +5V peak to ØV base. TP5 should now read about +3.65 VDC for a 3586B or +4.56 VDC for a 3586A so the rectified peaks of the signal should be tripping the comparator at twice the signal frequency at TP2 or 1000Hz (2 x 500Hz). Reducing the input signal peaks at TP4 below +3.65V (or +4.56V) should again shut off U19.

8-G-37. To check the Dead Timer and Impulse Counter circuits, use the following procedure.

1. Perform steps 1-4 of paragraph 8-G-36 to provide an input to the Dead Timer circuit. This should be a 1000Hz TTL square wave at U20(3).

2. Connect a scope to A70TP3 and select a sweep time/division that will trigger the sweep start at a 1Hz rate. Use DC coupling. The trace should be sweeping at about a +4.4 VDC level with 6-8 negative pulses visible to Ø VDC per sweep. (A 3586A should have 7 or 8 pulses visible per sweep and a 3586B should have 6 or 7 pulses).

3. Decrease the scope sweep speed to about .5 SEC/DIV.

4. Selectively look at U21 pins 3,2,6, and 7. In a 5 second period, the number of pulses present at each pin should agree with Table 8-G-5.

Table 8-G-5. Impulse Counter Maximum Output.

U21 Pin #	Pulses (5 Seconds)
3	18-20
2	9-10
6	5
7	3

8-G-38. To check the Dead Timer for its sensitivity to very short duration noise spikes, use the following procedure.

1. Disconnect the input signal source.

2. Press RECALL and Ø.

3. Noise floor in LO DIST should be less than −116dBm.

4. Connect the scope to A70TP3 (AC coupled), sweep rate at .2 SEC/DIV.

5. Select a THRESHOLD of −111dBm.

6. The resulting waveform at TP3 should resemble that shown in Figure 8-G-4 for the 2 second sweep duration.

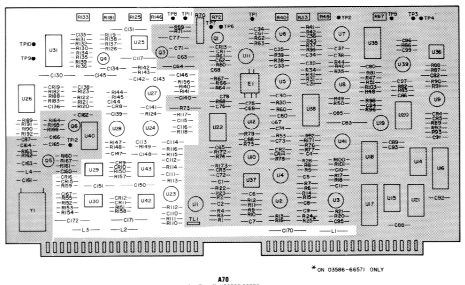
8-G-39. Impulse Error Codes.

8-G-40. Error code E 6.1 indicates that the current Threshold setting was less than −56dB below the Full Scale setting when START was pressed. This is an operator error. Increase the Threshold setting or decrease the Full Scale setting.

8-G-41. Error code E 6.2 indicates that the current Threshold setting was greater than +3dB above the Full Scale setting when START was pressed. This is an operator error. Decrease the Threshold setting or increase the Full Scale setting.

8-G-42. Calibration Oscillator Troubleshooting.

8-G-43. The Calibration Oscillator should have no output at TP12 unless U16(5) is HIGH (+4.3 VDC). When U16(5) is HIGH, TP12 should have a TTL square wave present at 1.6625MHz (3586B) or 1.6425MHz (3586A). U16(5) should be HIGH anytime CAL is active or TF2 is active (paragraph 8-58).



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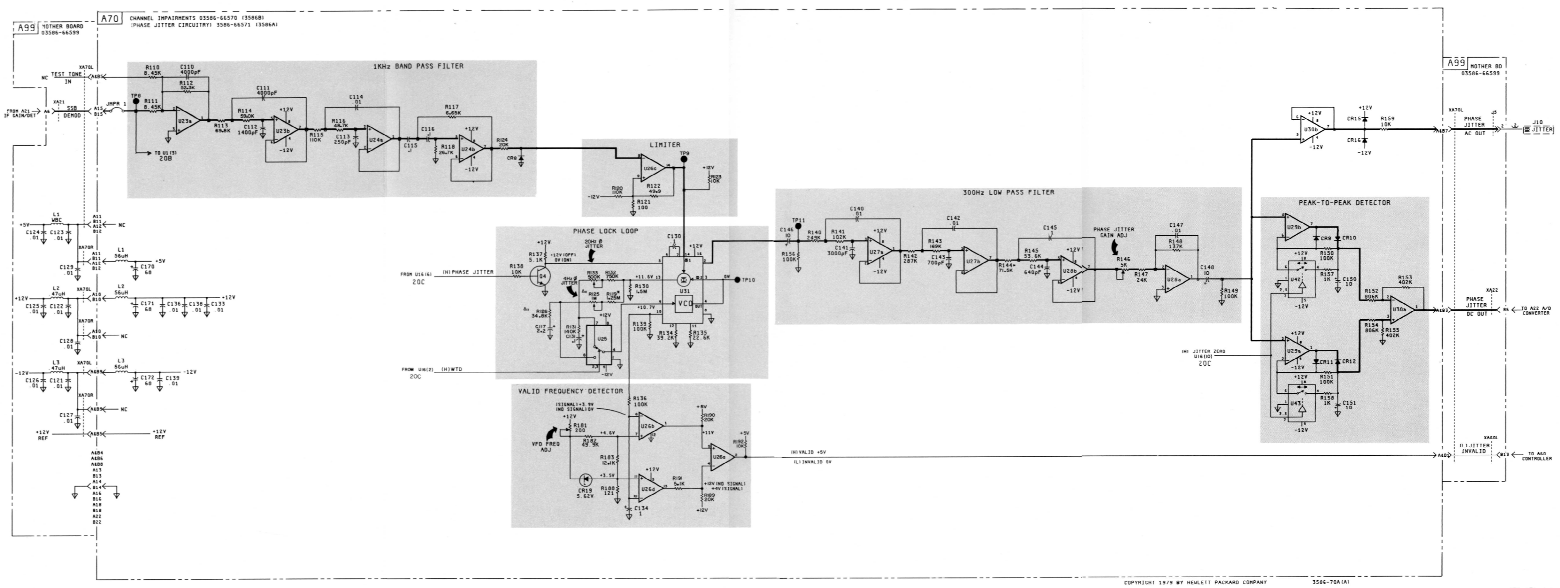
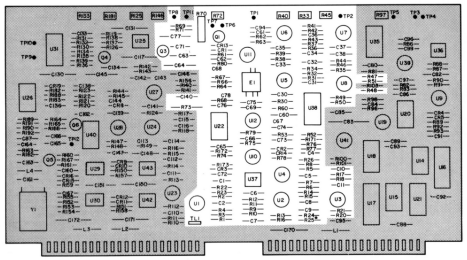


Δ11 Figure 8-G-1. Schematic - Phase Jitter Circuits (A70)
8-G-11/8-G-12



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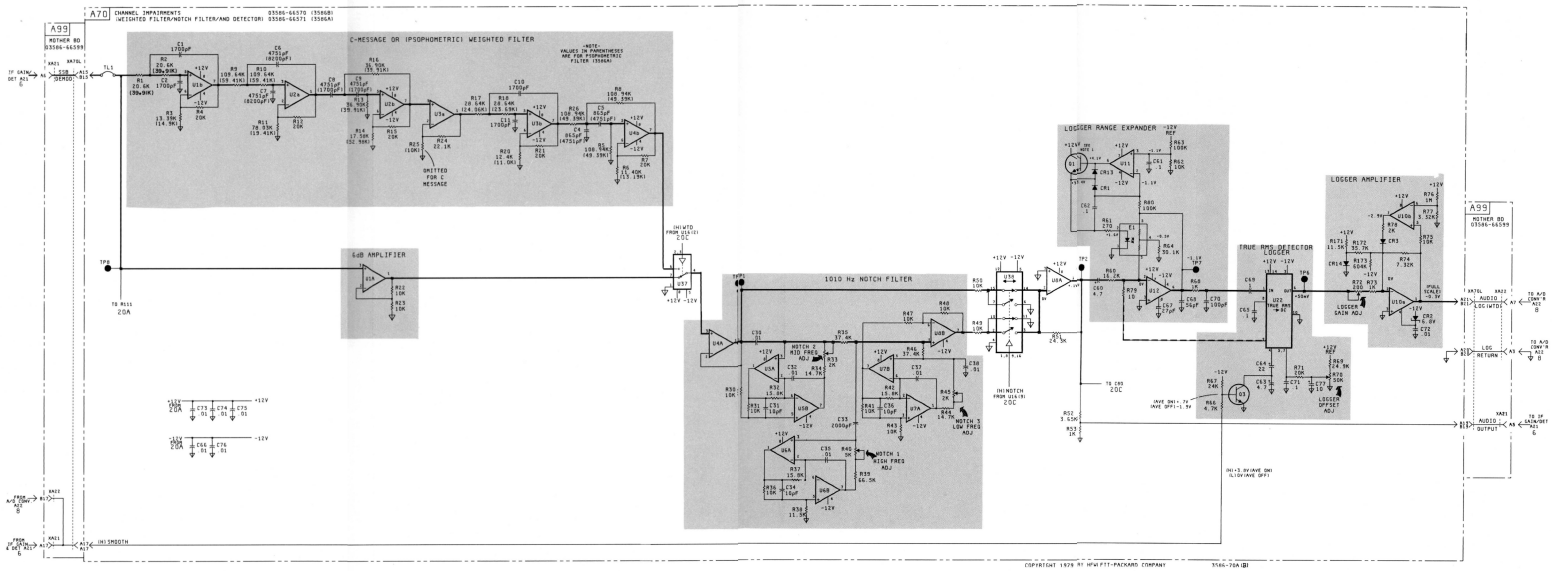
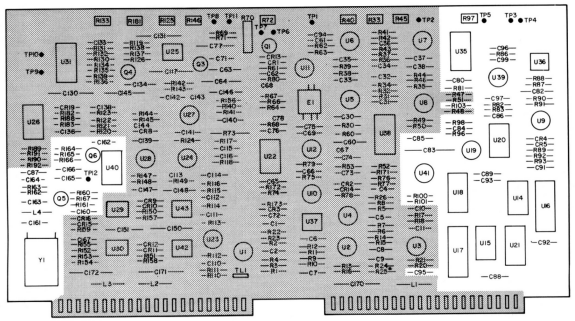


20B

Figure 8-G-2. Schematic - Weighted/Notch Filters (A70)



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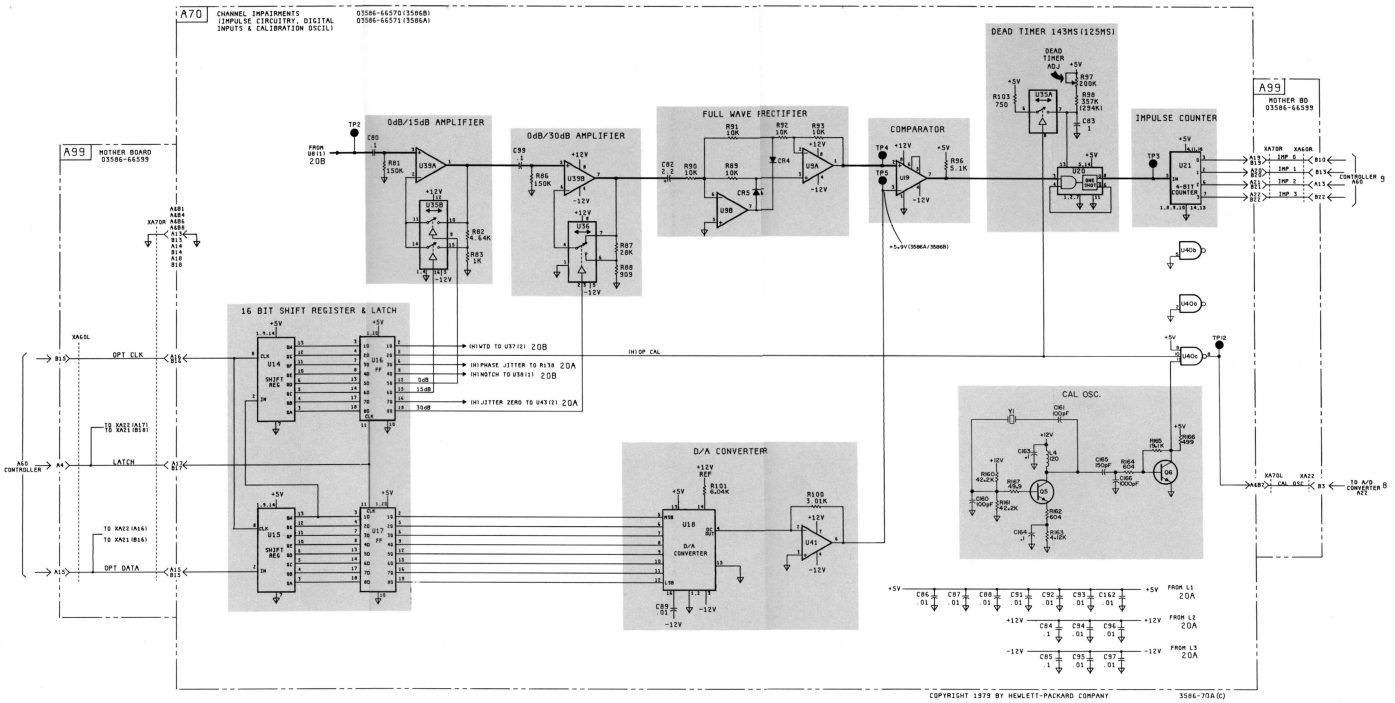
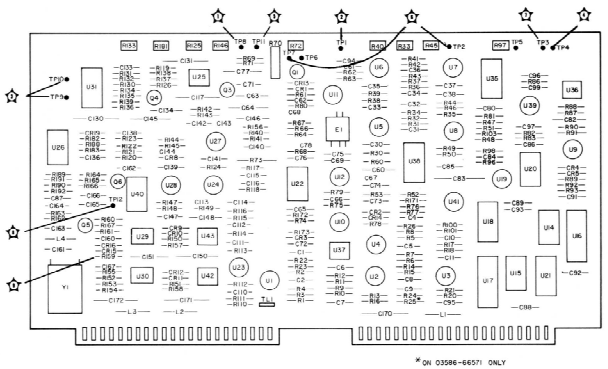


Δ11 Figure 8-G-3. Schematic - Impulse Noise Circuits (A70)



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hp Part No. 03586-66570
Rev D

Notes:

1. TEST TONE is used for engineering purposes only. A method of inputting two tones to simulate phase jitter for testing can be found in paragraph 8-G-18.

2. The signal voltage at TP7 is related to the voltage at TP2 as shown in Table 8-G-3. The table also shows corresponding voltages at TP6 and U10(1).

3. IMPULSE audio is always passed through the Notch Filter when IMPULSE is selected. If WTD 3100 is selected, it will also be passed through the Weighted Filter.

4. The signals shown at ϕ JITTER AC OUT and at ϕ JITTER DC OUT were obtained by using the special set-up procedure in paragraph 8-G-18. If no phase jitter is present on an input signal, these two outputs will both be zero. The Scale Factor for ϕ JITTER DC OUT is 6°/−1.0 volt. See also Note 7.

5. The signal at TP1, TP2, TP7, and TP4 was obtained by inputting a 1MHz signal at 0dBm with the following 3586 selections: ENTRY 100, F.S. = 0dBm, LO DIST, CARR, ↗1 (USB), 3100Hz, Frequency = 1MHz. The audio signal frequency is the difference between the second IF (15.625KHz) and the USB oscillator SSB LO frequency (17.475KHz) or 1850Hz. The rectified signal at TP4 has the negative peaks overlaid with the positive peaks and will read 3700Hz if a counter is connected to TP4. The voltages shown at TP6 and U10(1) are the corresponding DC full scale voltages obtained with a full scale 1850Hz signal (2.2Vp-p) present at TP8.

6. The waveform depicted in the sketch at TP3 was obtained by cycling power on the instrument, setting the IMPULSE threshold just above the noise floor (no input signal), and allowing random noise spikes to trigger the dead timer with the impulse time (start) running and WTD 3100Hz selected. The sketch represents negative pulses randomly occurring at approximately 7 counts/sec.

7. The waveforms shown at TP8, TP9, TP10, and TP11 were obtained by inputting a 1.001MHz signal at 0dBm with the following 3586 selections: ENTRY 100, F.S. = 0dBm, ϕ JITTER mode, Frequency = 1MHz, 3100Hz. The 1000Hz signal thus obtained is Full Scale at 2.2Vp-p. See also Note 4.

8. Voltages ±10%.

9. A table of digital values for the 15 possible voltage selections for D/A conversion can be found in Table 8-G-4.

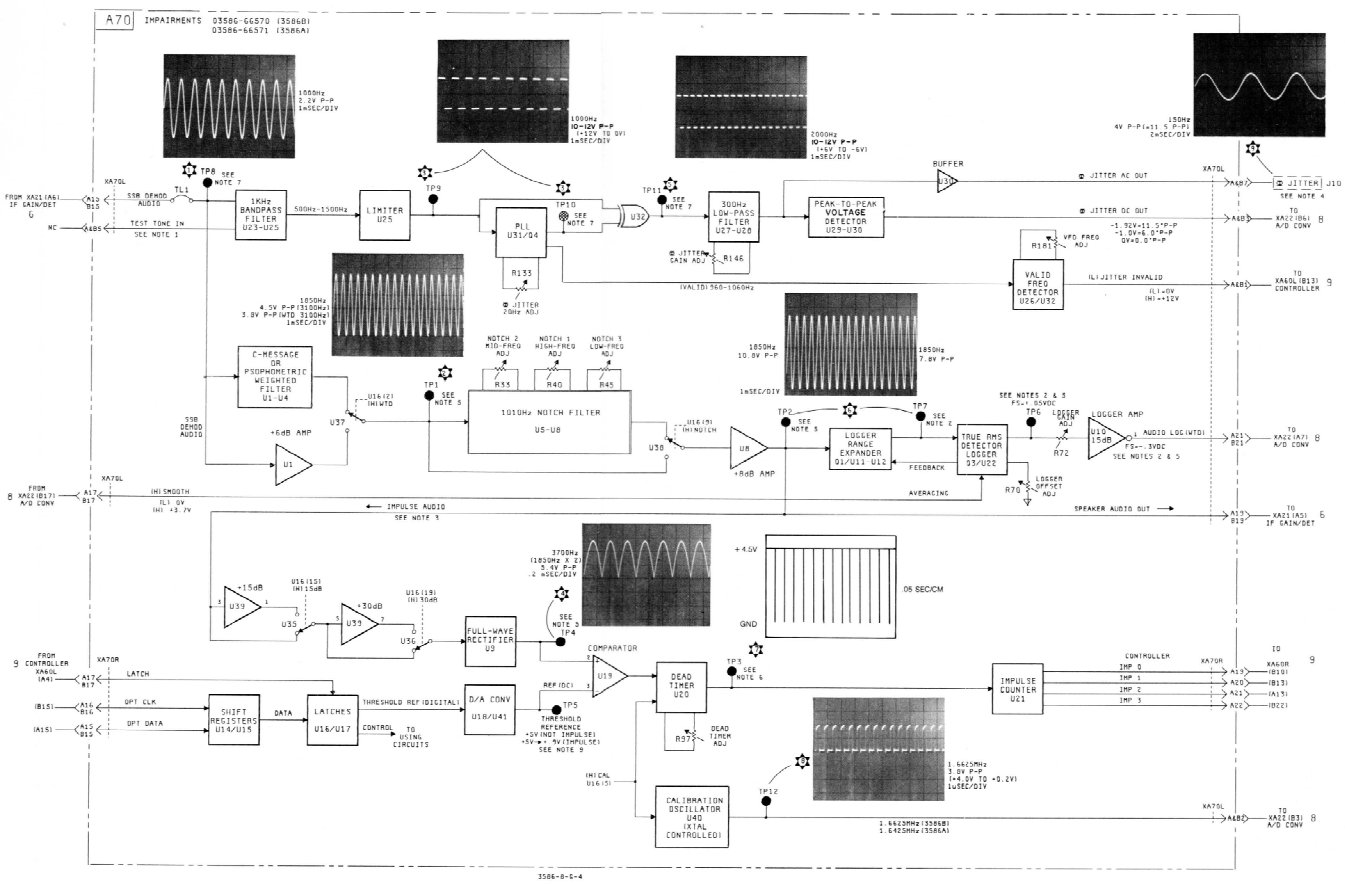

Figure 8-G-4. Functional Block - Impairments (A70)

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8-H-4.	Theory of Operation (Cross Reference)	8-H-1
8-H-5.	Frequency Reference (A40) - Paragraph 8-291	8-H-1
8-H-6.	10MHz Frequency Reference (A16) - Paragraph 8-304	8-H-1
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FREQUENCY REFERENCE
SERVICE GROUP H

Contents

Adjustments (Cross Reference)	Paragraph 8-H-1
Theory of Operation (Cross Reference)	Paragraph 8-H-4
Troubleshooting Data	Paragraph 8-H-7
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8-H-1. ADJUSTMENTS (CROSS REFERENCE).

8-H-2. Frequency Reference Adjustments (A40).

Designation	Adjustment Title	Paragraph
A40R78	50MHz Oscillator Frequency Adjust	5-4

8-H-3 10MHz Frequency Reference Adjustments (A16).

Designation	Adjustment Title	Paragraph
A16R7	Sense Offset Adjust	5-23
A16U3	10MHz Frequency Adjust	5-23

8-H-4. THEORY OF OPERATION (CROSS REFERENCE).

8-H-5. Frequency Reference (A40) - Paragraph 8-291.

8-H-6. 10MHz Frequency Reference (A16) - Paragraph 8-304.

8-H-7. TROUBLESHOOTING DATA.

8-H-8. A40 General Information.

8-H-9. There are two ways for the VCXO on the A40 board to lock up and provide a 50MHz reference frequency. It can do it on its own with no external reference, in which case the Phase Detector bridge circuit (CR50-53) is shut off and R78 sets the exact frequency of the VCXO. The other way is with an external reference signal which turns the bridge circuit on, allowing 10MHz from U53(4) to provide an input to U54(3). With this second method, the Lock Speed-up circuitry, in conjunction with the Phase Detector bridge, helps the VCXO to phase-lock to the external reference signal. The external reference must be 10MHz or an exact submultiple thereof (5MHz, 3.333 333MHz, 2.5MHz, 2MHz, or 1MHz).

8-H-10. The voltage at TP6 is the VCXO control voltage. Because of the high frequency (50MHz), and differences between individual component tolerances for the VARICAP diode CR91, the case capacitance of Y90, and transistors Q90 and Q91, the voltage at TP6 **could** be anywhere between −10V and +10V. (Usually, however, it will be in the range of Ø to +3V.) The crystal frequency may not be exactly 50MHz, therefore considerable adjustment range is provided by the gain of U54 (gain = 11 or approximately 20dB). The peak DC voltage into U54(3) would be about ±1 VDC if you could see it, but with filter components C56 and R59 maintaining the input to U54 at close to Ø volts, only the output voltage at TP4 provides an indication that the circuit is working. The voltage at TP4 should be constant when the VCXO is locked up although its range is about the same as that for TP6.

8-H-11. An important thing to remember about the Lock Speed-up Circuitry and the Unlock Detector is that they normally only function with an external reference input. If there is no external reference signal, you should never see an unlock condition (Error code "Err 8" displayed and A40DS1 lit). Also, if the external reference signal is present but very far off in frequency or too low in amplitude, the 3586 may not be locked to it and there will be no indication to tell the operator that the instrument is not frequency locked. The only time, therefore, that the unlock condition should exist is when there is a strong input signal at the EXT REF INPUT jack that is just far enough off in frequency that the board cannot lock to it. Under these conditions, the output of U54 at TP4 will not be a constant DC voltage but will be swinging positive and negative rapidly trying to find a signal it can lock to. The negative excursions will charge C75 negatively through CR55 which will bias FET Q55 off (it is normally on when the board is locked up). With Q55 off, the normal loop bandwidth of approximately 18Hz is expanded to about 1000Hz by adding another 5.1 Megohms of resistance (R88) to ground. This helps the loop to lock up quickly to a signal slightly off frequency by causing the VCXO to change frequency until the 10MHz frequency from U53 through the bridge shifts enough in phase to lock up to the external reference. At that time, the output of U54 should stop swinging, C75 will discharge, Q55 will again turn on and the loop should be locked up. While C75 is charged negative and the loop is unlocked, FET Q56 is also biased off, turning on Q54 and sending a (L) REF UNLOCKED signal to the controller (A60) to display error code Err 8. This LOW signal at TP3 also turns on DS1.

8-H-12. A40 Troubleshooting Hints.

8-H-13. The only convenient way to troubleshoot the VCXO is to short TP6 to ground. This should cause the VCXO to oscillate at some frequency close to 50MHz. If it does not, suspect A90 and Q91 first, then CR91, CR90, Y90, and U92.

8-H-14. If the VCXO oscillates near 50MHz with TP6 shorted to ground, but won't oscillate or drives to a different frequency when the short is removed and an external reference signal is present, disconnect the external reference. If the VCXO output is now correct, suspect the external reference source frequency first. It must be 10MHz or an exact submultiple of 10MHz such as 1MHz (÷10), 2MHz (÷5), 2.5MHz (÷4), 3.333333MHz (÷3) or 5MHz (÷2). If the external reference is not very close to one of these exact frequencies, the VCXO cannot lock to it.

8-H-15. If the reference frequency is correct, suspect Q50, Q51, CR50-53, U1 and U2. If the external reference signal is the correct frequency and is present at the bridge circuit then the problem may be no 10MHz at the collector of Q52. If the 10MHz is missing at Q52, ground TP6 again and trace the VCXO output around the loop to U53(7). You then should be able to trace the 10MHz from U53(4) through U52, U51 and Q52 to prove that they are working.

If the external reference and the 10MHz from Q52 are both present at the bridge, the problem must be in the Lock Speed-up circuitry. Suspect Q55 and Q56 first, then U54 and U55, finally CR54 and CR55.

8-H-16. R78 Adjustments. Because of the very slow loop speed for frequency changes, TP4 and TP5 should be shorted together to speed up VCXO reactions to adjustments of R78. Also, if adjustment of R78 is necessary, the service technician must anticipate the drift of the VCXO once the A40 board is put back in the cavity. Trial and error is the only method possible. Make an adjustment while the A40 is on an extender board, note the reading, reinsert the board in the cavity and note the drift. Then put the board back on the extender and compensate for the drift by setting the frequency an equivalent amount off in the opposite direction.

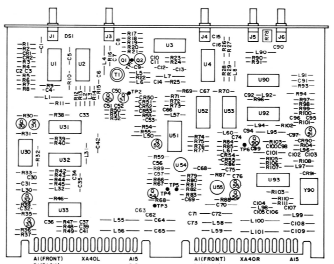
8-H-17. Spurious Signals. If an external reference signal is used which is not completely "clean" (free of noise or line frequency sidebands), these signals can be coupled onto the 50MHz reference frequency as "spurs". The exact frequency of the spurs riding on the 50MHz would be a function of the fundamental and whether the external reference is a $\div 1$, $\div 2$, $\div 3$, etc. submultiple of 10MHz.

8-H-18. Most of the "divide-by" circuits on the A40 board use ECL level signals. However, U33 converts the ECL to CMOS for circuits requiring the 1MHz output and Q30/Q31 convert ECL to TTL for the 100kHz output to A32.

8-H-19. High residual phase jitter problems (see paragraph 8-G-16) could be caused by Y90, Q55, or Q56. Y90 can also be a cause of the 50MHz not adjusting correctly with R78.

8-H-20. A16 Troubleshooting Hints.

8-H-21. The A16 is a fairly straightforward board to troubleshoot. Check XA16(A7) for +23V and TP3 for +15V (regulated from U1). If they are there, U3 should be oscillating. If not, check A1 and Q2 for shorts. U2 could prevent the 10MHz from leaving the board by incorrectly sensing a cold oven when the instrument is actually warmed up, especially if R7 is misadjusted. The 10MHz output is not a perfect sine wave. Some harmonic distortion is normally present (see Figure 8-H-3 for a typical waveform at J1). TP1 and TP2 are mismarked (reversed) on the PC board (Rev. A) and probably won't be corrected unless a major circuit change occurs. The silkscreen labels on the aluminum top cover, however, are correct.



A40
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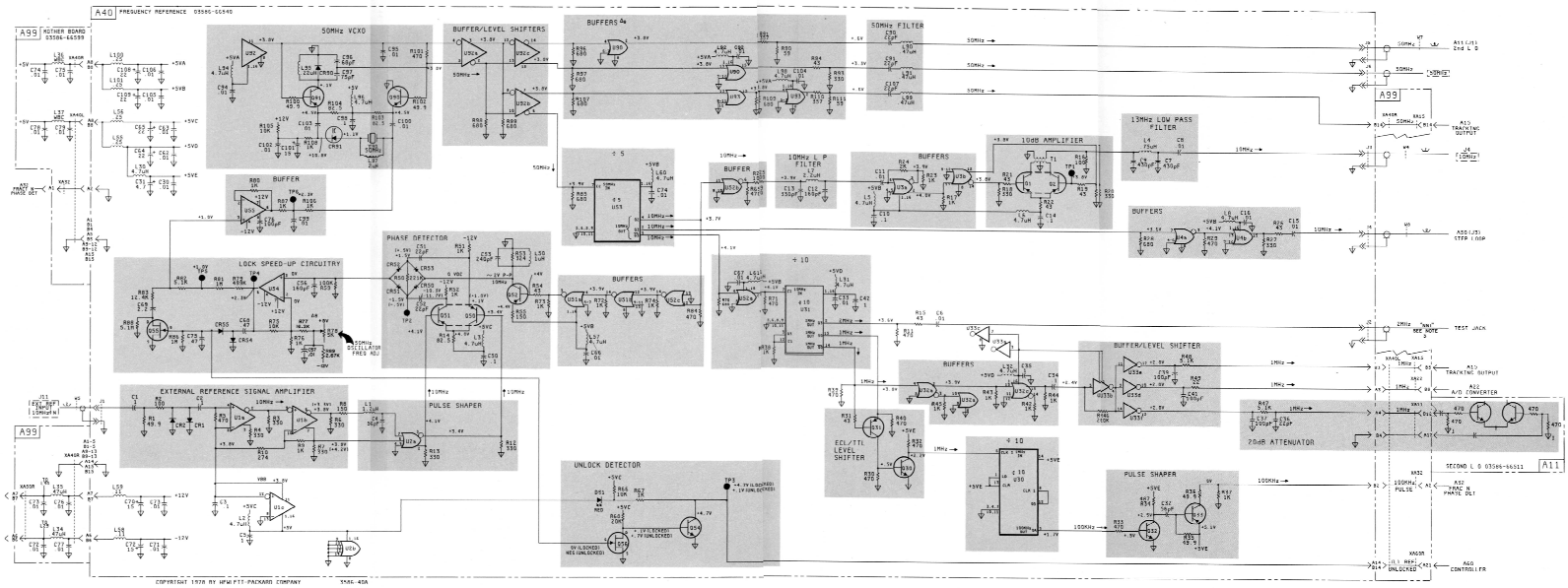
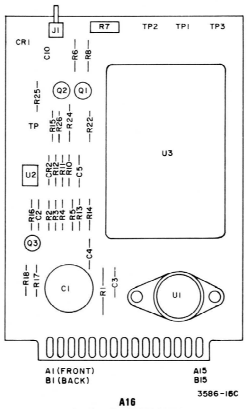
Rev B

3586-40C

NOTES

1. Voltages are ± 10% except for voltages at TP4, TP5, and TP6. These can vary from −10V to +10V when the VCXO is locked up at 50MHz as a function of individual circuit component tolerances for CR81, Y80, Q80 and Q91.
2. Voltages in ( ) are with no external frequency reference applied to A40J1. Otherwise, voltages were taken with a 10MHz external source (A16-Option 004) applied to the EXT REF INPUT jack A40J1.
3. Not normally installed.





A16
-hp- Part No. 03586-66516
Rev A

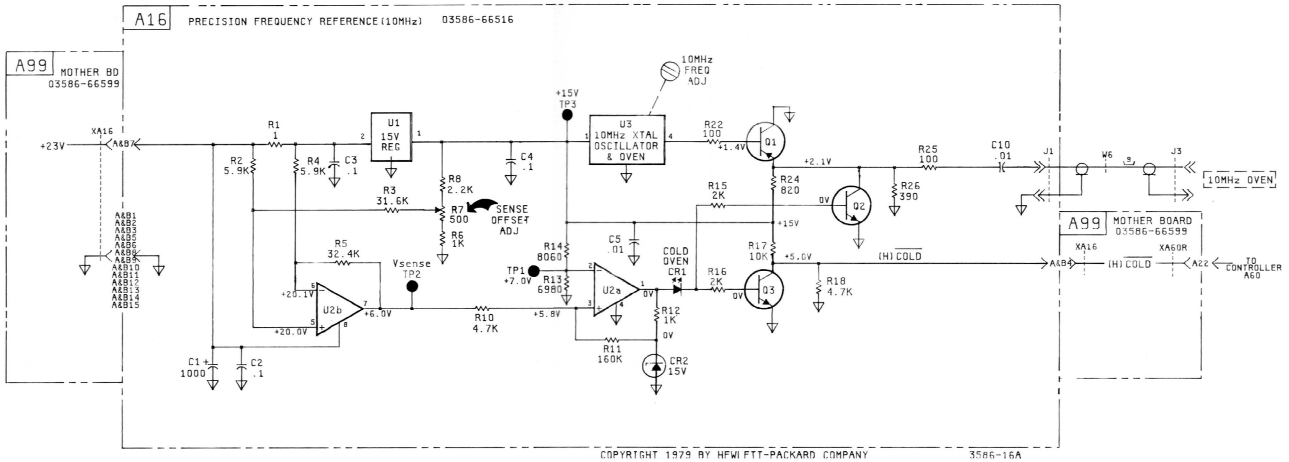
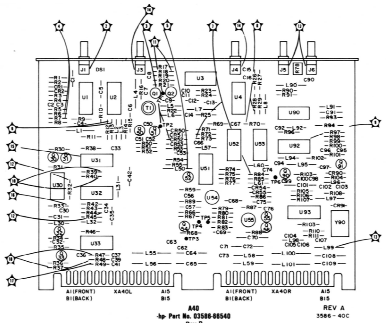
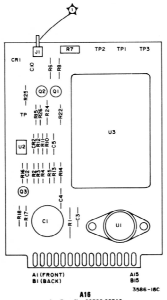


Figure 8-H-2. Schematic - 10MHz Frequency Reference (A16)
8-H-7/8-H-8





NOTES:

1. A16R7 is adjusted when the oven is cold so that the voltage at TP2 equals the voltage at TP1 plus 0.3 VDC.
2. Adjust A16U3 frequency when oven is warm to 10,000,000.0Hz.
3. Any external reference input equal to 10MHz divided by an integer (N) from 1 to 5 (or 10) may be used. Signal shown is 10MHz from A16.

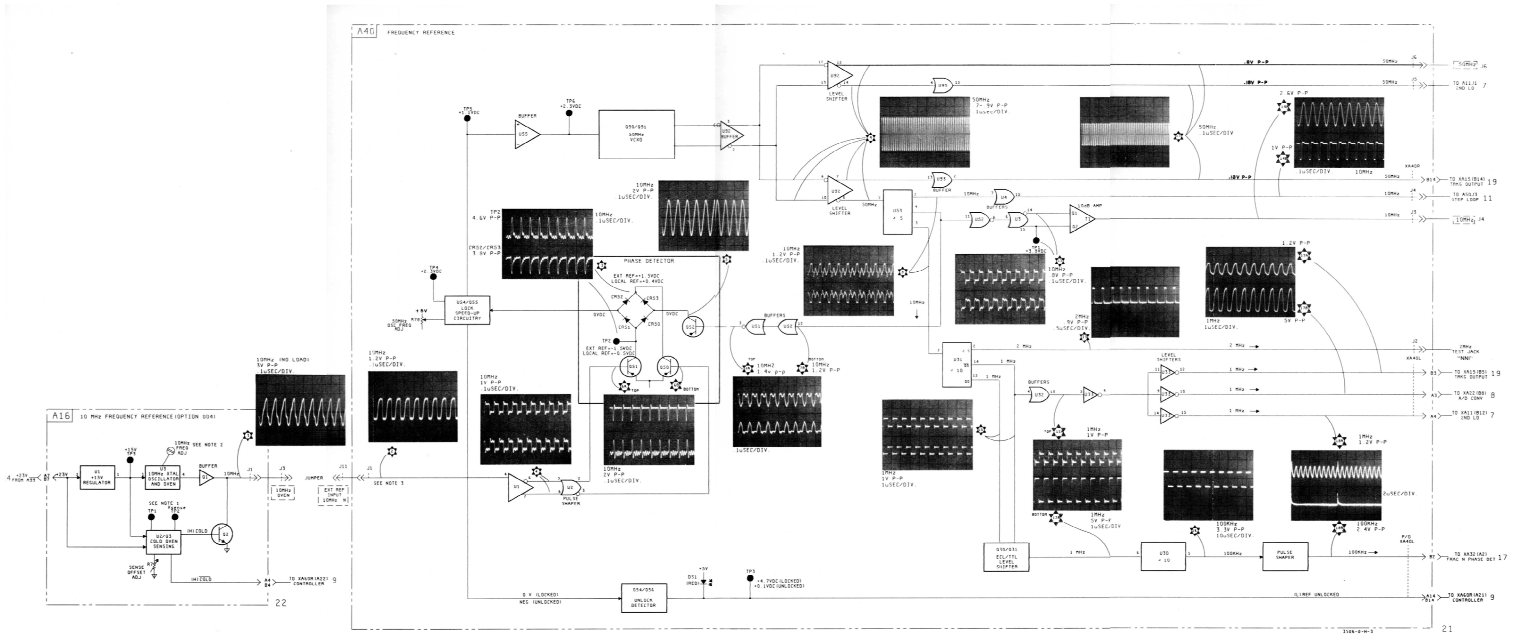


Figure 8-H-3. Functional Block - Frequency Reference (A40/A16)

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HP-IB
SERVICE GROUP I

Contents

Troubleshooting Data	Paragraph 8-I-1
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Function Diagram (A61)	Figure 8-I-4
Theory of Operation (Reference)	Paragraph 8-306

8-I-1. TROUBLESHOOTING DATA.

8-I-2. HP-IB Hardware.

8-I-3. The HP-IB hardware in the 3586 consists of the A61 printed circuit board, a small printed circuit board (A62) mounted on the rear panel and a blue 34-wire cable connecting the two P.C. boards. A61 has all the logic circuits for HP-IB operation and A62 has the address select switch (A62S1) and the standard 24 pin HP-IB bus receptacle (A62J1) for interfacing with other HP-IB - capable instruments. See Figure 8-I-1.

8-I-4. A62S1 is a seven contact DIP switch which is used to select the 3586A/B/C HP-IB address and also selects certain test/operate modes of the instrument. A62S1 contacts are open (1) (HIGH) when in the up position and closed (Ø) (LOW) when in the down position.

NOTE

If contacts 1 or 2 on A62S1 are in the down (Ø) position, normal HP-IB operation with an HP-IB system controller is not possible.

A62S1

Switch Contact	Schematic Label	Use
1	NORMAL (1)/TEST (Ø)	Selects normal operating mode (open) or test (HP-IB signature analysis) mode (closed).
2	REMOTE (1)/TRACK (Ø)	Selects HP-IB REMOTE (open) or tracking generator (TALK only) mode (closed).
3	A4	Address - 16 (MSB)
4	A3	Address - 8
5	A2	Address - 4
6	A1	Address - 2
7	AØ	Address - 1 (LSB)

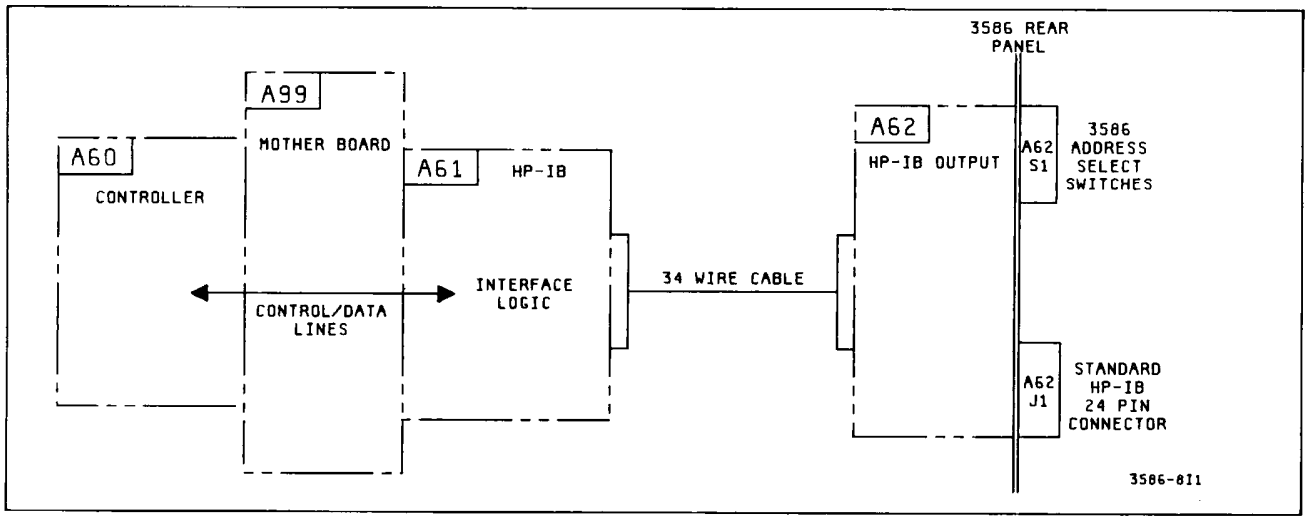


Figure 8-I-1. 3586 HP-IB Hardware Interface.

8-I-5. 3586A/B/C HP-IB Address

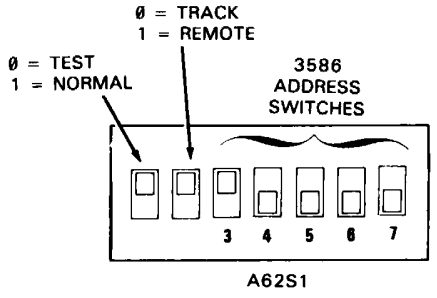
8-I-6. The 3586A/B/C is shipped with an HP-IB address of 16. This would be selected with the following switch set-up:

Switch Contact	Address Value	Contact Position	Circuit Application
3	16	1 (up)	open = +5v = HIGH
4	8	0 (down)	closed = GRD = LOW
5	4	0 (down)	closed = GRD = LOW
6	2	0 (down)	closed = GRD = LOW
7	1	0 (down)	closed = GRD = LOW

Refer to Table 8-I-1 for address selection codes. The standard ASCII code software addresses for the 3586A/B/C are: TALK = "P"(01010000) LISTEN = Ø (zero) (00110000).

Table 8-I-1. Address Selection.

ASCII Code Character		Address Switches					5-bit Decimal Code	
Listen	Talk	A5	A4	A3	A2	A1		
SP	@	0	0	0	0	0	00	
!	A	0	0	0	0	1	01	
"	B	0	0	0	1	0	02	
#	C	0	0	0	1	1	03	
$	D	0	0	1	0	0	04	
%	E	0	0	1	0	1	05	
&	F	0	0	1	1	0	06	
'	G	0	0	1	1	1	07	
(	H	0	1	0	0	0	08	
)	I	0	1	0	0	1	09	
*	J	0	1	0	1	0	10	
+	K	0	1	0	1	1	11	
,	L	0	1	1	0	0	12	
-	M	0	1	1	0	1	13	
.	N	0	1	1	1	0	14	
/	O	0	1	1	1	1	15	
0	P	1	0	0	0	0	16	← 3586A/B/C
1	Q	1	0	0	0	1	17	
2	R	1	0	0	1	0	18	
3	S	1	0	0	1	1	19	
4	T	1	0	1	0	0	20	
5	U	1	0	1	0	1	21	
6	V	1	0	1	1	0	22	
7	W	1	0	1	1	1	23	
8	X	1	1	0	0	0	24	
9	Y	1	1	0	0	1	25	
:	Z	1	1	0	1	0	26	
;	[	1	1	0	1	1	27	
<	\	1	1	1	0	0	28	
=	]	1	1	1	0	1	29	
>	~	1	1	1	1	0	30	



8-I-7. Tracking Generator Mode.

8-I-8. Switching A62S1 (2) to the TRACK or Ø (down) position puts the 3586A/B/C into the "TALK only" mode. It may then control the frequency of a tracking generator such as the 3336A/B/C or the 3335A. When the 3586 is in the TRACK mode, the ability to "talk" to the tracking generator (which must be in the "LISTEN only" mode) is controlled by the front panel LOCAL key. This turns the communication to the tracking generator on or off as indicated in the FREQUENCY/ENTRY display area. Pressing MEASurement CONTinue restores frequency display when "ON" or "OFF" is displayed. When A62S1 (2) is in the REMOTE or 1 (up) position, the 3586 may talk and listen for normal HP-IB use.

NOTE

The 3586 sends a listen address of 00100 (4) when it is in the "TALK only" mode. Since the 3335A does not have a "LISTEN only" mode, the address set on the 3335A rear panel HP-IB address switches must be set to 00100 in order for the 3335A to track the 3586 in frequency.

8-I-9. When an HP-IB controller is not available, use of the 3586 Tracking Generator mode can establish whether the eight data lines (DI01-DI08) are functional and also if the 3586 can set the DAV, ATN and REN lines.

8-I-10. The HP-IB bus uses "LOW = true" logic where LOW = Ø volts and HIGH (false) = +3.5 volts. In REMOTE, with nothing connected to the rear panel HP-IB connector, all the active (non-grounded) pins on the HP-IB connector (see Figure 8-I-2) will be HIGH (pins 1-11 and 13-17). When A62S1 (2) is placed in TRACK (down), pins 1-4, 11, 13 and 14 will go LOW. If a scope is now used to observe the HP-IB data and control lines while changing the frequency of the 3586, the following pins will be seen to "wiggle": pins 1-4, 6,11, 13-15, and 17. Use a slow sweep speed (e.g., 5 milli-seconds) on the scope and turn the FREQUENCY TUNE (RPG) control with AUTO or FREQ STEP selected to change the frequency and see the pulse trains. NOTE: The pulses are only present while the frequency is changing.

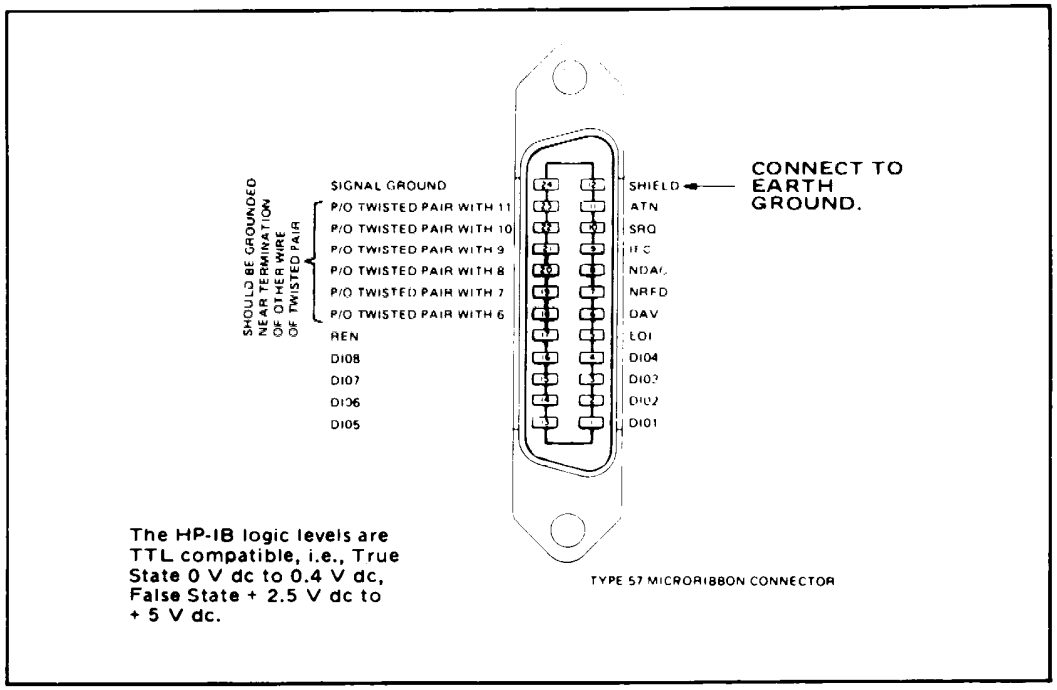


Figure 8-I-2. HP-IB Connector (A62J1).

8-I-11. HP-IB Problem Symptoms.

8-I-12. 3586 HP-IB problems manifest themselves in several ways.

1. If no communication at all can be obtained between an HP-IB controller and the 3586, the problem could be:

a. Incorrect address on 3586 (hardware) or on Controller (software).

b. External cables not fully connected or corrosion on HP-IB connector pins.

c. External cables too long (see paragraph 8-I-23 for maximum cable lengths allowed).

d. HP-IB System Controller defective.

e. A61 board (3586) not fully seated or corrosion on edge connector pins.

f. Cable from A61 to rear panel not fully seated on A61.

g. Damaged cable from A61 rear panel.

h. A61 malfunction.

i. A60 malfunction.

2. If intermittent communication over the bus can be obtained, verify whether the 3586 is at fault by trying another instrument with the system controller or another controller with the 3586. Intermittent HP-IB operation could be caused by:

a. External cables not making good connection or corrosion on HP-IB connector pins.

b. External cables too long (see paragraph 8-I-23 for maximum cable lengths allowed).

c. HP-IB System Controller defective.

d. A61 board (3586) not fully seated or corrosion on edge connector pins.

e. Cable from A61 to rear panel not fully seated on A61.

f. Damaged cable from A61 to rear panel.

g. A61 malfunction.

h. A60 malfunction.

3. If communication over the bus appears to be solid with respect to the **transfer** of data, but there are occasional or repetitious errors in the data, the problem could be caused by:

a. A data line stuck HIGH or LOW at the 3586 or at the system controller.

b. A bad HP-IB interconnect cable (open or shorted).

c. A61 malfunction.

d. A60 malfunction.

8-I-13. Preliminary HP-IB Troubleshooting.

8-I-14. Before getting involved with troubleshooting circuits on the A61 board, perform the following checks to verify that the A61 board is the most probable cause of an existing HP-IB problem:

1. Verify your set-up is correct and functional:

   a. Correct hardware (3586) and software (system controller) addresses must be selected. They must be identical.

   b. Cable connectors should be fully seated.

2. Substitute where possible:

   a. Try a different system controller.

   b. Try another instrument with the system controller.

   c. Try another interconnect cable.

   d. Try another A61 board in the 3586.

   e. Try another A60 board in the 3586.

3. Inside the 3586:

   a. Verify that the A61 board is fully seated.

   b. Make sure the cable from the A61 board to the rear panel is not physically damaged and that its connector is fully seated on the A61 board.

   c. Verify that the A60 board is fully seated.

4. Disconnect the exterior HP-IB cable from the 3586 and check that functional operation is normal using the front panel keys in the LOCAL mode.

8-I-15. Bus Analyzer Troubleshooting.

8-I-16. If a Hewlett-Packard 59401A Bus System Analyzer is available, it may be used to help identify a "stuck high", "stuck low", or intermittent data/control line(s) on the HP-IB bus. Follow the instructions in the 59401A Operating Manual for use of this analyzer.

8-I-17. Signature Analysis (SA) Troubleshooting.

8-I-18. The best method for troubleshooting a known problem on the A61 board is to use SA on the logic circuits associated with the failed data/control line(s). Before beginning, however, it is a good idea to verify that the HP-IB problem really is on the A61 board. Follow the steps in paragraph 8-I-14 to ensure that the A61 board is the most probable cause of an existing HP-IB problem.

8-I-19. Remove power from the 3586. Disconnect the cable from A61. Remove the A61 board and install an extender board in its place. Solder an electrolytic capacitor (value range = 2.2μF to 10.0μF) in the two unused holes on the PC board adjacent to A61U1 pin 4 (+ end of the capacitor) and pin 10 (− end). Be sure to remove this capacitor at the completion of SA testing. Now place A61 on the extender board and reconnect the cable. Select A62S1 (1) to the TEST or Ø (down) position, A62S1(2) to the TRACK or Ø (down) position and set A62S1 (3-7) to 10001. These switches place the A61 board in a self-test mode where the microprocessor (A61U1) generates specific periodic digital signatures on the data control lines.

8-I-20. Connect a 5004A Signature Analyzer to A61 as follows:

Clock - A61TP1 (Falling edge)
Start - A61TP5 (Rising edge)
Stop - A61TP5 (Falling edge)
Ground - 3586 main frame

8-I-21. Remove the A60 board during A61 SA testing to avoid excessive wear of the input relays on A2. Apply power to the 3586. Check the +5V signature with the 5004A probe. It should be 4CCF. If the +5V signature is not 4CCF, cycle the POWER switch on the 3586 one or more times until 4CCF is obtained. If 4CCF cannot be obtained for the +5V signature, the microprocessor (U1) on A61 may be bad. Put a scope on Test points TP1-TP5 and look for the correct signals as shown on Figure 8-I-3 and Figure 8-I-4.

8-I-22. If 4CCF is obtained for the +5V signature, proceed as follows:

1. If the HP-IB problem has already been isolated to one or more data/control lines being bad using the procedures found in paragraphs 8-I-10 and 8-I-16, it will only be necessary to check the signatures on logic circuits associated with those particular lines. Refer to Table 8-I-3 for signatures to check for known bad data/control lines.

2. If no previous isolation has been performed, check the signatures on all of the data/control lines at the rear panel HP-IB connector (A62J1), as shown in Table 8-I-3. If one or more of the signatures are bad, use the pin connections shown in the table for that line to locate the bad component(s).

3. If the problem appears to be that *all* of the data/control lines are not operating correctly, begin with the processor signatures (U1) in Table 8-I-2. Then check for the correct signatures on the ROM (U29) if the processor is good.

4. If the problem is just one of erroneous data being transferred, check the signatures on the data lines (DI01-DI08) at the HP-IB connector on the rear panel (A62J1 pins 1-4 and 13-16) to see if one of them is stuck high or low. If yes, use Table 8-I-3 to trace the logic circuits back to the processor.

8-I-23. HP-IB Cable Length Restrictions.

8-I-24. To achieve design performance with the HP-IB and, especially, to prevent intermittent operation or even total failure, proper voltage levels and timing relationships must be maintained. If the system cable is too long, the lines cannot be driven properly and the system will fail to perform. Standard HP-IB cable lengths are:

-hp- 10631A	3 feet
-hp- 10631B	6 feet
-hp- 10631C	12 feet

8-I-25. Therefore, when interconnecting an HP-IB system, it is important to observe the following rules:

a. The total cable length for the system must be less than or equal to 20 meters (65 feet).

b. The total cable length for the system must be less than or equal to 2 meters (6 feet) times the total number of devices connected to the bus.

8-I-26. These are important points to remember since up to 15 HP-IB compatible instruments may be interconnected at one time in the system. If the total cable length for the system as defined above is exceeded, poor system performance could be obtained, falsely indicating an instrument failure. For example, if there are three devices on the HP-IB bus, the maximum cable length is 18 feet (3 x 6). If you are using two each 12-foot cables to connect the three instruments (piggy-backing the cables at one instrument), the total length is 24 feet and poor system performance may result.

Table 8-I-2. HP-IB Signatures.

U1

	1	40	4CCF
#4CCF	2	39	6P60
#0000	3	38	2676
4CCF	4	37	AC30
4CCF	5	36	P712
9H99	6	35	F8U4
4CCF	7	34	PP37
#4CCF	8	33	31PH
#4CCF	9	32	815A
#4CCF	10	31	7U34
#0000	11	30	PH06
1A4F	12	29	5A60
U467	13	28	AAUC
2119	14	27	1H1P
82AC	15	26	4CCF
64AU	16	25	4CCF
P190	17	24	4CCF#
H2AC	18	23	2AA1
P73C	19	22	U5A8
0000	20	21	4CCF#

U2

1H1P	1	16	4CCF
1H1P	2	15	AC30
1H1P	3	14	AC30
5C71/C6P2	4	13	AC30
AAUC	5	12	0000
AAUC	6	11	5A60
AAUC	7	10	5A60
0000	8	9	5A60

U3

PH06	1	16	4CCF
PH06	2	15	2676
PH06	3	14	2676
5C71/C6P2	4	13	2676
7U34	5	12	0000
7U34	6	11	815A
7U34	7	10	815A
0000	8	9	815A

U4

31PH	1	16	4CCF
31PH	2	15	P712
31PH	3	14	P712
5C71/C6P2	4	13	P712
PP37	5	12	5C71/C6P2
PP37	6	11	F8U4
PP37	7	10	F8U4
0000	8	9	F8U4

U5

14C6	1	16	4CCF
14C6	2	15	A5HP
14C6	3	14	A5HP
0000	4	13	A5HP
4CCF	5	12	0000
4CCF	6	11	UC32
4CCF	7	10	UC32
0000	8	9	UC32

U6

8PPF	1	14	AAUC
5A60	2	13	1H1P
4CCF	3	12	0000
4CCF	4	11	1H1P
5A60	5	10	4CCF
F550	6	9	AAUC
4CCF	7	8	4CCF

U7

AAUC	1	14	5A60
1H1P	2	13	AC30
4CCF	3	12	0000
4CCF	4	11	AC30
1H1P	5	10	4CCF
4CCF	6	9	5A60
AAUC	7	8	4CCF

U8

7U34	1	14	815A
PH06	2	13	2676
4CCF	3	12	0000
4CCF	4	11	2676
PH06	5	10	4CCF
4CCF	6	9	815A
7U34	7	8	4CCF

U9

PP37	1	14	F8U4
31PH	2	13	6P60
4CCF	3	12	0000
4CCF	4	11	6P60
31PH	5	10	4CCF
4CCF	6	9	F8U4
PP37	7	8	4CCF

U10

P712	1	14	PP37
F8U4	2	13	31PH
4CCF	3	12	0000
4CCF	4	11	31PH
F8U4	5	10	4CCF
4CCF	6	9	PP37
P712	7	8	4CCF

U11

03AA	1	14	7U34
815A	2	13	PH06
4CCF	3	12	0000
4CCF	4	11	PH06
815A	5	10	4CCF
4816	6	9	7U34
4CCF	7	8	4CCF

U12

A5HP	1	14	0000
UC32	2	13	14C6
4CCF	3	12	0000
4CCF	4	11	14C6
UC32	5	10	4CCF
4CCF	6	9	0000
A5HP	7	8	4CCF

U13

0000	1	14	C08P
5UOA	2	13	
4CCF	3	12	0000
14C6	4	11	
4CCF	5	10	
4CCF	6	9	4CCF
4CCF	7	8	UC32

U14

UH5P	1	16	4CCF
AAUC	2	15	UH5P
AAUC	3	14	1H1P
5A60	4	13	1H1P
5A60	5	12	815A
PH06	6	11	815A
PH06	7	10	7U34
0000	8	9	7U34

Table 8-I-2. HP-IB Signatures (Cont'd).

U15

UH5P	1	16	4CCF
F8U4	2	15	C6P2
F8U4	3	14	AC30
31PH	4	13	AC30
31PH	5	12	2676
PP37	6	11	2676
PP37	7	10	
0000	8	9	

U16

	1	14	4CCF
	2	13	0000
C727	3	12	4CCF
UF9C	4	11	0000#
#4CCF	5	10	4CCF#
#0000	6	9	5UOA
0000	7	8	14C6

U17

UH5P	1	14	4CCF
0000	2	13	9H99
C6P2	3	12	0000
4816	4	11	H625
2676	5	10	F550
UH5P	6	9	UH5P
0000	7	8	AC30

U18

	1	14	4CCF
	2	13	8PPF
	3	12	6P60
	4	11	AC30
	5	10	6P60
	6	9	03AA
0000	7	8	2676

U19

#0000	1	14	4CCF
UF9C	2	13	4CCF
#4CCF	3	12	UH5P
C727	4	11	C6P2
#0000	5	10	0000
4CCF	6	9	4CCF#
0000	7	8	4CCF

U20

14C6	1	14	4CCF
3F3U	2	13	0000
H625	3	12	4CCF#
0000	4	11	0000
C08P	5	10	
0000	6	9	
0000	7	8	4CCF

U21

4CCF	1	20	4CCF
POA2	2	19	05U7
1A4F	3	18	P73C
U467	4	17	H2AC
FC5C	5	16	51H5
3U97	6	15	51H5
2119	7	14	P190
82AC	8	13	64AU
8445	9	12	5635
0000	10	11	4CCF#

U22

4CCF	1	20	4CCF
C727	2	19	UH5P
05U7	3	18	POA2
51H5	4	17	FC5C
9FUU	5	16	C6P2
3F3U	6	15	HA10
51H5	7	14	3U97
5635	8	13	8445
3H52	9	12	08CA
0000	10	11	4CCF#

U23

4CCF	1	20	4CCF
FACO	2	19	CU24
1A4F	3	18	P73C
U467	4	17	H2AC
F20A	5	16	44F5
C938	6	15	5H17
2119	7	14	P190
82AC	8	13	64AU
PF4C	9	12	0807
0000	10	11	4CCF#

U24

4CCF	1	20	4CCF
1A4F	2	19	P73C
	3	18	
	4	17	
U467	5	16	H2AC
2119	6	15	P190
	7	14	
	8	13	
82AC	9	12	64AU
0000	10	11	

U25

	1	14	4CCF
	2	13	4CCF
	3	12	0000
	4	11	3H52
	5	10	4CCF#
	6	9	
0000	7	8	

U26

#4CCF	1	20	4CCF
4CCF	2	19	4CCF#
1A4F	3	18	4CCF
0000	4	17	P73C
U467	5	16	0000
0000	6	15	H2AC
2119	7	14	0000
0000	8	13	P190
82AC	9	12	4CCF
0000	10	11	64AU

Table 8-I-2. HP-IB Signatures (Cont'd).

U27

4CCF	1	16	4CCF
C08P	2	15	
2AA1	3	14	
0000	4	13	
#4CCF	5	12	
5UOA	6	11	
U5A8	7	10	
0000	8	9	

U28

	1	16	4CCF
	2	15	A5HP
	3	14	PP62
	4	13	4CCF#
2AA1	5	12	U5A8
	6	11	
UC32	7	10	14C6
0000	8	9	0000#

U29

05U7	1	24	4CCF
51H5	2	23	4CCF#
51H5	3	22	U5A8
5635	4	21	4CCF
8445	5	20	0000
3U97	6	19	2AA1
FC5C	7	18	4CCF#
POA2	8	17	P73C
1A4F	9	16	H2AC
U467	10	15	P190
2119	11	14	64AU
0000	12	13	82AC

U30

UC32	1	16	4CCF
0000	2	15	5U21/4CCF#
4CCF	3	14	3141/25HF
	4	13	9FUU
3141/25HF	5	12	0000
6P60	6	11	4CCF
5U21/HCCF#	7	10	
0000	8	9	

U31

9FUU	1	14	5C71/C6P2
	2	13	
4CCF	3	12	0000
	4	11	
	5	10	
4CCF	6	9	C6P2
9FUU	7	8	4CCF

A62J1 HP-IB Connector

1-1H1P	5-P712	9-4CCF	13-7U34	17-14C6	21-0000
2-AAUC	6-F8U4	10-A5HP	14-815A	18-0000	22-0000
3-5A60	7-AC30	11-UC32	15-31PH	19-0000	23-0000
4-PH06	8-2676	12-0000	16-PP37	20-0000	24-0000

NOTES:

1. All the above signatures are valid only when the SA test for A61 as described in paragraphs 8-I-19 through 8-I-22 is performed.

2. The +5V signature is 4CCF. Ground (ØV) is 0000.

3. # means that the probe tip flashes on signatures associated with +5V (4CCF) and ground (0000). If # is not present on 4CCF or 0000, the probe tip lamp should not flash.

4. Pins where no signature is indicated are either not used or are disconnected when A60 is removed for the A61 SA test.

5. Pins where two signatures are shown, either is correct.

6. Signatures are valid for both Rev. A and Rev. B versions of ROM U29.

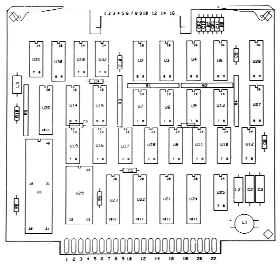
Table 8-I-3. HP-IB Circuits (By Line).

Data/Control Line Label	HP-IB Pin No.	IC Pins To Check*	DSA Test Signature**
DIO1	A62J1(1)	U1(27),U6(13),U2(1),U7(2)	1H1P
DIO2	(2)	U1(28),U6(14),U2(7),U7(1)	AAUC
DIO3	(3)	U1(29),U6(2),U2(9),U7(14)	5A60
DIO4	(4)	U1(30),U11(13),U3(1),U8(2)	PH06
DIO5	(13)	U1(31),U11(14),U3(7),U8(1)	7U34
DIO6	(14)	U1(32),U11(2),U3(9),U8(14)	815A
DIO7	(15)	U1(33),U10(13),U4(1),U9(2)	31PH
DIO8	(16)	U1(34),U10(14),U4(7),U9(1)	PP37
DAV	(6)	U1(35),U10(2),U4(9),U9(14)	F8U4
NRFD	(7)	U1(37),U17(10)#,U6(1)##,U18(11),U2(15),U7(13)	AC30(#F550)(##8PPF)
NDAC	(8)	U1(38),U17(4)#,U11(1)##,U18(8),U3(15),U8(13)	2676(#4816)(##03AA)
IFC	(9)	U26(14)#,U12(14)#,U5(7),U13(1)#,U27(5)	4CCF(#0000)
ATN	(11)	U1(23)#,U28(7),U12(2),U5(9),U13(14)##	UC32(#2AA1)(##CO8P)
REN	(17)	U1(22)#,U28(10),U12(13),U5(1),U13(2)##	14C6(#U5A8)(##5UOA)
SRQ	(10)	U1(24)#,U28(15),U12(1)	A5HP(#4CCF)
EOI	(5)	U1(36),U10(1)	P712

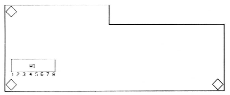
* If the correct signature is not present for any one of these pins, refer to the schematic (Figure 8-I-3), locate the indicated logic chip and the failed pin, and check all signatures on all logic chips connected to that line (Table 8-I-2). This should help to identify the failed chip. If it does not, replace all chips connected to the failed line, one at a time.

** Signatures are valid for both Rev. A and Rev. B versions of ROM U29.

#
Signatures with these symbols apply only to pins with these symbols.



A61
-hp- Part No. 03586-66561
Rev C



A62
-hp- Part No. 03586-66562
Rev B

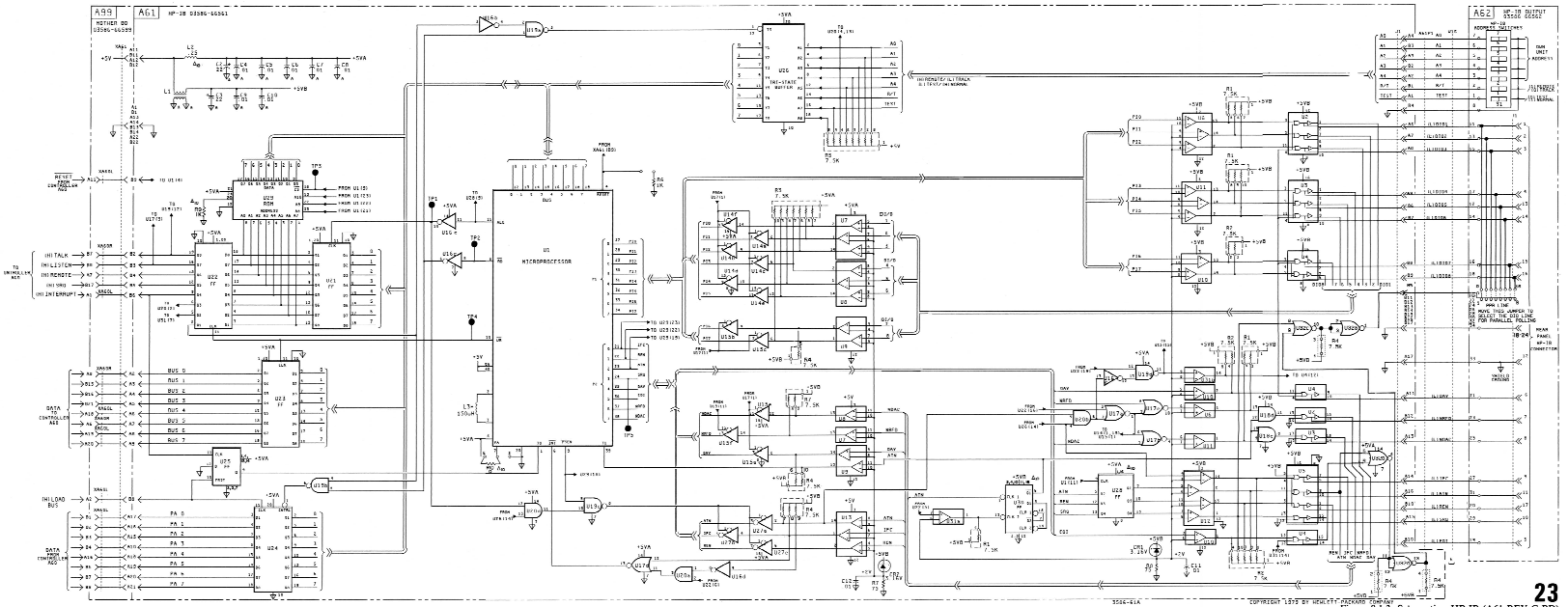
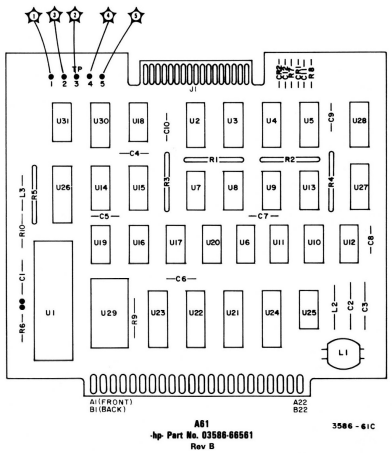


Figure 8-1-3. Schematic - HP-IB (A61 REV C BD)
(A62 REV B BD)
8-1-13/8-1-14



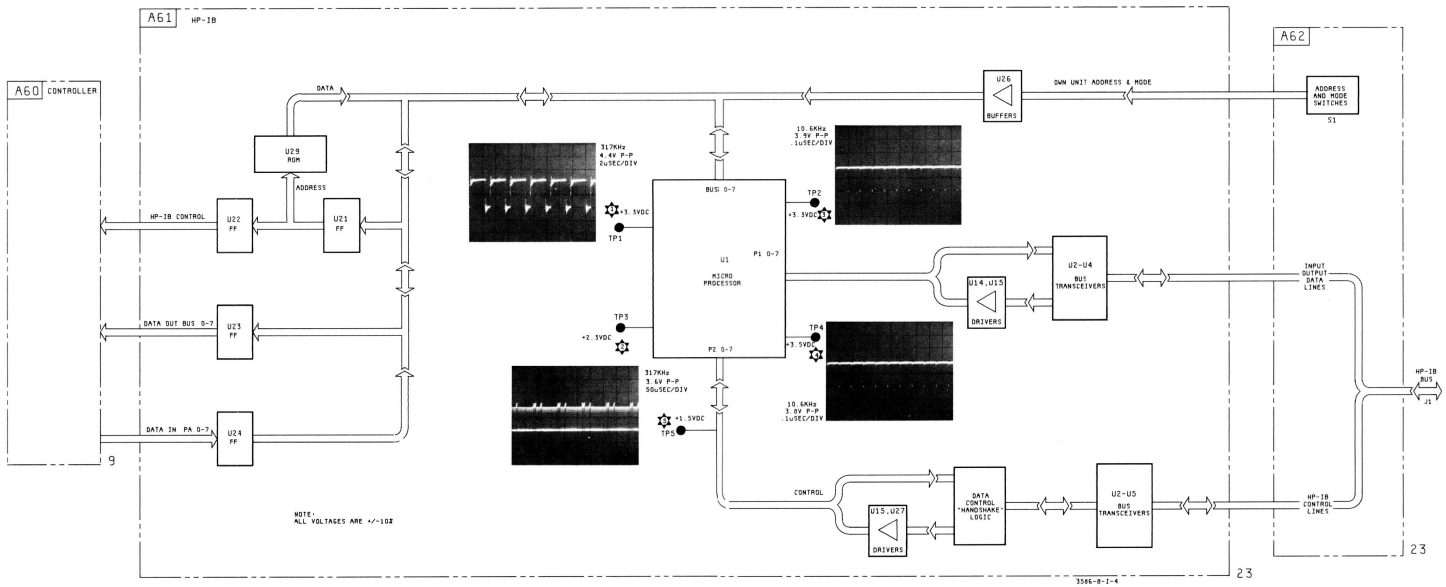


Figure 8-I-4. Functional Block - HP-IB (A61/A62)

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POWER
SERVICE GROUP J

Contents

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Troubleshooting Data	Paragraph 8-J-4
Schematic Diagram	Figure 8-J-4
Functional Block Diagram	Figure 8-J-5

8-J-1. ADJUSTMENTS.

8-J-2. There is only one adjustment for the power supplies. A80R15 adjusts the + 12 V supply and the + 12V is then used as a voltage reference for the other two main supplies (– 12V and + 5V). The procedure for adjusting A80R15 is as follows.

1. Check that the + 12, – 12, and + 5 volt green L.E.D.'s on A80 are lit. If not, proceed to paragraph 8-J-5.

2. Connect a DVM to A80TP1 (+ 12V); configure it to measure dc.

3. Adjust A80R15 such that the DVM reads from + 11.990 volts dc to + 12.010 volts dc.

4. Check that A80TP2 is – 12 volts dc ± 30mV.

5. Check that A80TP3 is + 5.250 volts dc ± 100mV.

6. If either 4 or 5 are false, then repeat steps 3 through 5 as necessary.

8-J-3. If A80R15 cannot be adjusted such that all three regulated supplies (+ 12, – 12, and + 5 volts) can be brought into tolerance at the same time, place A80 on an extender board and troubleshoot the problem voltage supply using the voltage references on the schematic (Figure 8-J-4).

8-J-4. TROUBLESHOOTING DATA.

8-J-5. A80 Red/Green LED Indicators.

8-J-6. The three green LED's should always be lit. Each one indicates that its respective voltage (+ 12V, – 12V, or + 5V) is **close** to its normal operating setting. If the respective red LED is lit for any voltage, it indicates that current limiting is taking place for that particular voltage and a short is quite likely somewhere on that bus.

8-J-7. If the +12V bus is shorted to ground, the following conditions will exist with the POWER switch in the ON position:

1. The front panel will be dark.

2. All of the A80 LED's will be dark except the +12V red LED.

3. A80 TP1, TP2, and TP3 voltages will be less than 100 milli VOLTS.

4. The fan (B1) will be running.

8-J-8. If the −12V bus is shorted to ground, the following conditions will exist with the POWER switch in the ON position:

1. A4 "overload" red LED will be lit.

2. A53 "unlock" LED will be lit.

3. A80 red LED for −12V will be lit.

4. A80 green LED's for +12V and +5V will be lit provided they are not shorted also.

5. A31 "unlock" LED will be lit.

6. A11 "unlock" LED will be lit.

7. Front Panel indications will be OVLD flashing, intermittent error codes in the MEASUREMENT/ENTRY display area, and either 3586 in the FREQUENCY/ENTRY display area (short present at turn-on) or the last selected frequency present (short occurred after turn-on).

8. TF13 will fail all steps.

9. TF14 will pass.

8-J-9. If the +5V bus is shorted to ground, the following conditions will exist with the POWER switch in the ON position:

1. The front panel will be dark.

2. A4 "underload" LED will be lit.

3. A80 red LED for +5V will be lit.

4. A80 green LED's for +12V and −12V will be lit provided they are not shorted also.

5. Meter M1 will be pegged full-scale.

8-J-10. AC Ripple Problems.

8-J-11. Excessive ripple on the supply voltages, especially the +5V regulated supply, can cause many different problem symptoms. If the processor appears to be continually resetting

itself and/or the front panel LED's and indicators are flickering constantly or continually changing their presentation, check for AC ripple as follows:

1. Using a DVM, verify the DC supply voltages on A80 are +12.000 VDC ± 10 millivolts at TP1, −12.000 VDC ± 30 millivolts at TP2 and +5.250 VDC ± 100 millivolts at TP3. If not, proceed to paragraph 8-J-1.

2. Verify that the AC ripple voltage at TP1, TP2, and TP3 is less than 25 millivolts RMS.

3. Using a scope, check TP1, TP2, and TP3 for the presence of any high frequency spurs riding the DC levels with amplitudes greater than 100 millivolts p-p. There should be none.

8-J-12. Ripple on the +5V supply is a likely cause of flickering front panel displays or erratic processor operation. If A80TP3 shows excessive ripple, replace A80U3. If A80U3 does not correct the problem it is probably being caused by CR20 or Darlington transistor Q3, both located on the Darlington transistor assembly. To replace these components it is necessary to remove the rear panel. Proceed to paragraph 8-J-14 for rear panel removal instructions.

NOTE

If the instrument serial number is 1927A-00122 or below, 11928A-00113 or below, 1929A-00102 or below, ripple on the +5V supply might be caused by the 5.6V Zener (CR20) that was installed in these serials (Part Number 1902-1232). Replacing CR20 with the current 6.2V Zener (Part Number 1902-1217) may correct the problem. Reference Figure 8-J-4.

8-J-13. If the +12V or −12V test ponts (TP1 and TP2 respectively) on A80 show excessive ripple, try changing A80U1 or A80U2 first. If that does not correct the problem, the associated Darlington transistor is probably bad. Proceed to paragraph 8-J-14 for rear panel removal instructions.

8-J-14. Rear Panel Removal.

8-J-15. To remove the rear panel for access to fuses A99F1-F4 and all power supply components not located on the A80 board, perform the following steps. (Reverse the steps for re-installation.)

WARNING

Disconnect line power cord before removing rear panel to prevent personal injury and accidental shorting of electrical components.

1. Remove top and bottom instrument covers.

2. If Option 004 is installed, remove the A16 board (2 screws and 1 cable).

3. Disconnect all coax cables from printed circuit boards that go to rear panel BNC connectors.

4. Remove the HP-IB connector from the rear panel (2 screws).

5. Remove the clear plastic protective shield above power transformer T1 (1 screw).

6. Remove the 4 top and 4 bottom screws holding the rear panel to the frame.

7. Disconnect A99J5 (5 pin connector) to rear panel BNC connectors.

8. Disconnect in-line connector (2 pins) from S3 to rear panel.

9. Disconnect A99J2 (14 pin connector) to T1.

10. Remove rear panel. (See Figure 8-J-1 for rear panel component identification.)

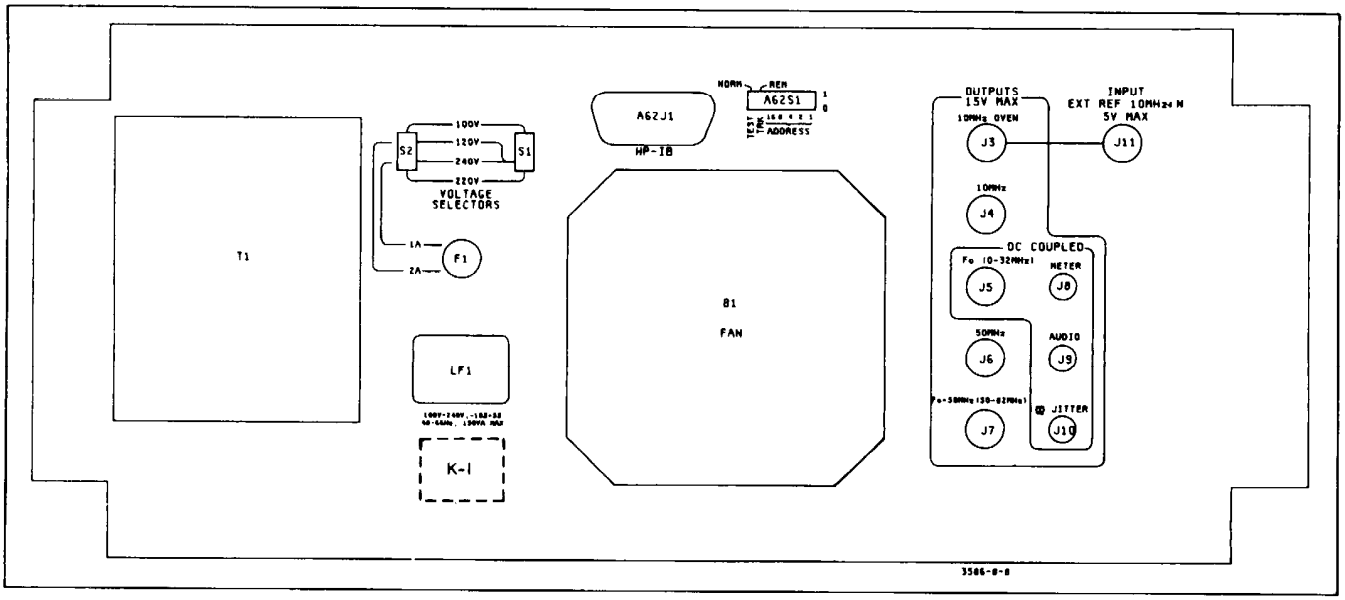


Figure 8-J-1. Rear Panel.

8-J-16. Darlington Transistor Assembly Removal.

8-J-17. To remove the Darlington transistor assembly, perform the following steps. (Reverse the steps for re-installation.)

1. Remove the rear panel (paragraph 8-J-14).

2. Remove the three screws holding the clear plastic cover over the plenum chamber and remove the cover.

3. Remove the two screws holding the Darlington assembly to the chassis and remove the plastic strip that separates the assembly from the chassis.

4. Disconnect A99J3 (13-pin connector) and remove the assembly.

5. Remove the two screws holding the heat shield in place on the assembly for access to Q1, Q2, Q3, CR20, and S3. (See Figure 8-J-2 for component identification.)

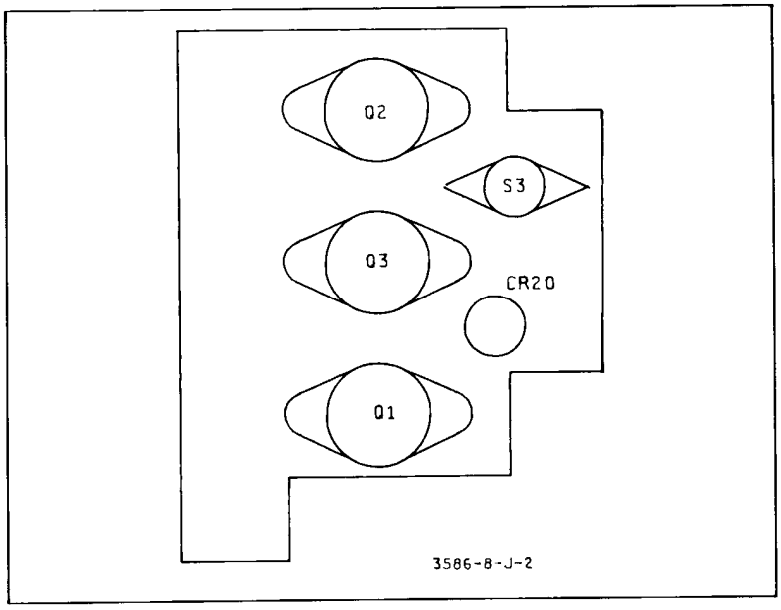


Figure 8-J-2. Darlington Transistor Assembly.

8-J-18. Troubleshooting Hints.

8-J-19. If the front panel is dark **and the fan does not run** when the POWER switch is in the ON position, but line fuse F1 is good, perform the following steps.

1. Inspect the power cord and power cord receptacle for damage.

2. Verify proper setting of the line voltage selector switches (S1 and S2) on the rear panel and check that the switches are fully making contact (in detent).

3. Remove the top cover.

4. Remove the two screws holding the HP-IB connector assembly (A62) to the rear panel and lay the assembly off to the side.

WARNING

The next step exposes line voltage within the instrument. Use care to avoid personal injury and/or shorting line voltage to ground or to adjacent components.

5. Remove the single screw that holds the clear plastic protective shield over T1 to the rear panel and remove the shield.

6. Connect one lead of a DVM (set to measure the appropriate input AC line voltage) to frame (chassis) ground.

7. With the other lead of the DVM, check for the presence of line voltage at S3 (solid gray wire). If not present, problem is in S3 or the in-line connector, the fuseholder, or line filter LF1. S3 should always be making contact unless ambient temperature exceeds about 105°C (221°F).

8. If line voltage is present at the output of S3, check for the presence of line voltage on the white/green/gray wire connecting S1 to S2. If not present, S1 or S2 or one of the primary windings of T1 is bad. If present, then A98S300 (POWER switch) is bad or the cable between A98J2 and A99J1 is bad or disconnected. The only things common to **both** a dark front panel and the fan not running (when F1 is good and POWER is ON) are input line power and the ground provided by A98S300. If one is present, the other must not be. Therefore, if all components check good, there must be a break in the wiring somewhere.

8-J-20. If the front panel is dark **and the fan is running** when the POWER switch is ON, perform the following steps.

1. Check the +12V, −12V, and +5V test points on A80. If they are all good, then either A60 or A98 is bad or the cable between A60J3 and A98J1 is disconnected or broken.

2. If the +12V supply is bad, it will affect both the −12V and the +5V supplies. The problem could be anywhere between T1 (and including T1) up to TP1 and including a short somewhere on the bus. (See paragraph 8-J-5 for information on the green and red LED's on A80.)

3. If the +12V, −12V, and +5V are missing, set the POWER switch to STBY and disconnect line voltage from the instrument. Go to step 10.

4. If just the +5V is missing, set the POWER switch to STBY and disconnect line voltage from the instrument.

5. Remove A80 and check for the present of a short to chassis ground at XA80(A20). If a short is present, remove all PC boards listed under +5V in Table 8-J-1, one-at-a-time, until the short disappears. Normal resistance of XA80(A20) to chassis ground is about 11 ohms (with or without A80 installed).

6. If a short is not present at XA80(A20) with A80 removed, remove the clear plastic shield covering power transformer T1 (one screw).

WARNING

The next step will expose line voltage within the instrument. Use care to avoid personal injury and/or shorting line voltage to ground or to adjacent components.

7. Reconnect line voltage to the instrument and set POWER to ON. Do **not** reinstall A80 yet.

8. Measure the AC voltage at pins 4 and 8 of T1 to chassis ground. They both should read about 4-5V RMS to ground. If the voltage is bad, go to step 9. If the voltage at T1(4) and T1(8) is good, remove the bottom cover and measure the voltage on the plus (+) terminal of

C3 with respect to the (−) terminal (chassis ground). It should read about +11 to +12 volts DC. (Refer to Figure 8-J-3 for the location of C3). If the voltage on C3 is bad, suspect CR5-CR8, C3, K1, Q3 and CR20. If the voltage on C3 is good, remove power, reinstall A80 and reapply power. The voltage on C3 should now be +8 to +9 VDC. If not, suspect Darlington Q3, CR20, A80U3, or other components on A80 in the +5V circuit.

9. If the voltage at T1(4) and T1(8) is bad, suspect T1, C6, CR5-CR8, K1 and C3. Remove the bottom cover for access to these components (refer to Figure 8-J-3).

10. If the +12V supply (TP1) is missing, remove power and take A80 out of the instrument. Check XA80(A4) for a short to chassis ground. If a short is present, remove all PC boards listed under +12V in Table 8-J-1, one-at-a-time, until the short disappears. If no short exists, remove the bottom cover and refer to Figure 8-J-3 for the following steps.

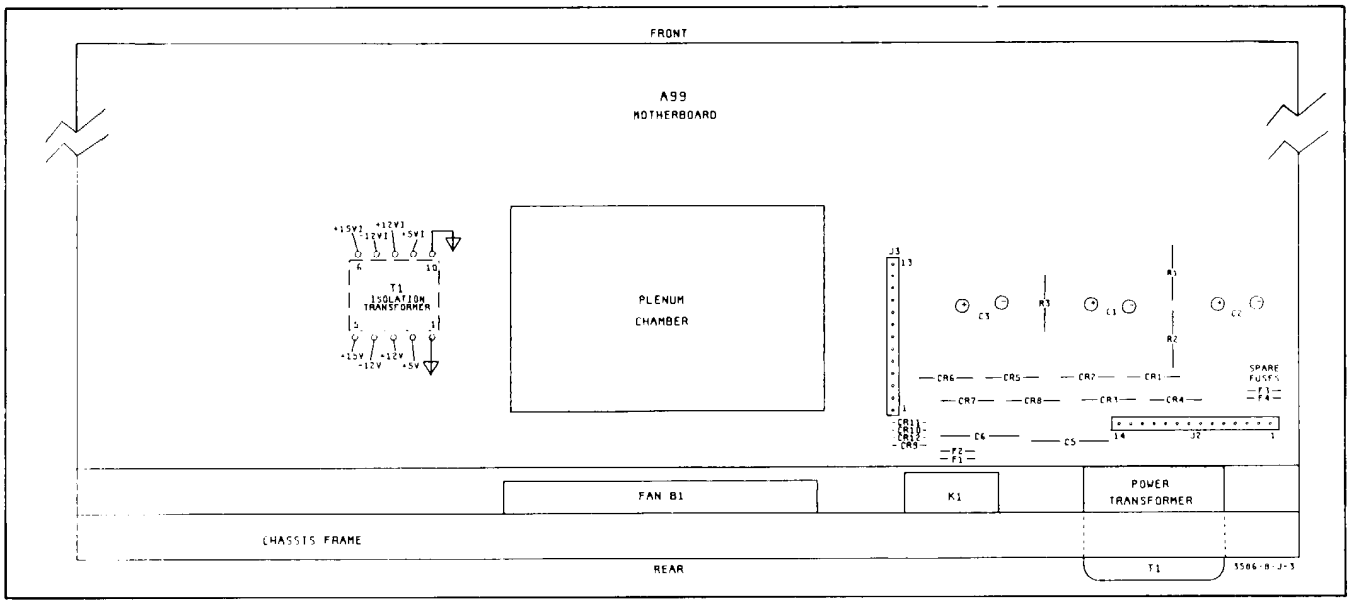


Figure 8-J-3. A99 Power Supply Components (Bottom View).

WARNING

The next step will expose line voltage within the instrument. Use care to avoid personal injury and/or shorting line voltage to ground or to adjacent components.

11. Reconnect line voltage to the instrument and set POWER to ON. Do not reinstall A80 yet.

12. Measure the AC voltage at J2(7) and J2(8) with respect to chassis ground. They both should read about 15-16 VRMS to ground. If the voltage is bad, go to step 13. If the voltage is good, measure the DC voltage across C1. It should read +20 to +21 volts DC. If the voltage on C1 is bad, suspect C1, CR1-CR4, Q1 and even possibly C2 and Q2. If the voltage on C1 is good, remove power, reinstall A80 and reapply power. The voltage on C1 should now be +18 to +19 VDC. If not, suspect Darlington Q1, A80U1 or other components on A80 in the +12V circuit.

13. If the voltage at J2(7) and/or J2(8) is bad, suspect T1, C5, CR1-CR4, C1 and C2.

8-J-21. Failure of the −12V supply by itself will not cause the front panel to be dark. However, if the −12V is missing or incorrect, it is possible to troubleshoot the −12V supply in the same manner as the +12V supply. Refer to paragraph 8-J-20 steps 10-13 for the procedure and Figure 8-J-4 for the −12V supply components and circuits.

8-J-22. If the front panel is lit up and appears to be functional but the fan does not run, suspect K1 or the fan itself (B1).

8-J-23. If the +23V or −23V unregulated voltages are missing, suspect fuses A99F1 and A99F2. Remove the bottom cover to check these fuses (see Figure 8-J-3 for locations). If either fuse is blown, spare fuses (F3 and F4) are provided. The rear panel must be removed to change the fuses (refer to paragraph 8-J-14 for removal procedures).

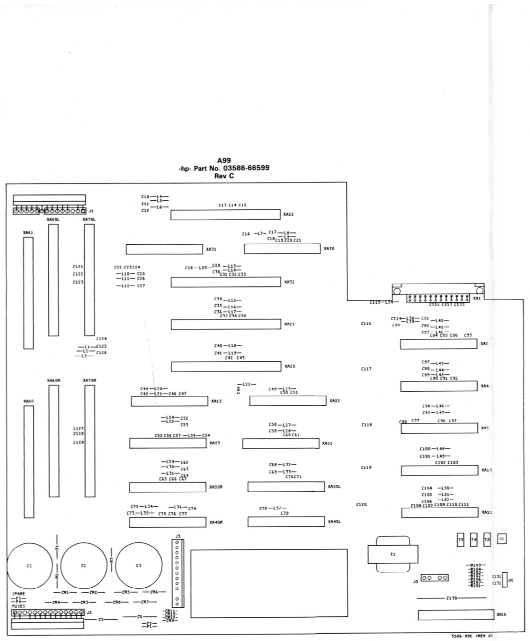
8-J-24. To help locate power supply shorts, Table 8-J-1 provides a DC voltage pin-out for each of the supply voltages.

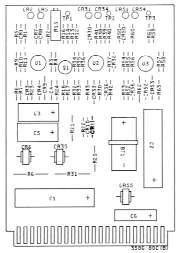
Table 8-J-1. 3586 DC Supply Voltage Pin-Outs.

+12VDC (Regulated) Origin: XA80 (A4-5, B4-5)	XA1 (A6, B6)* XA2 (A7, B7)* XA4 (A7, B7)* XA5 (A7, B7)* XA10 (A7, B7)* XA11 (A7, B7)* XA15 (A7, B7) XA20 (A10, B10) XA21 (A10, B10) XA22 (A10, B10) XA30 (A7, B7) XA31 (A7, B7)	XA32 (A10, B10) XA40R (A7, B7) XA50L (A7, B7) XA50R (A7, B7) XA51 (A7, B7) XA52 (A7, B7) XA53 (A7, B7) XA70L (A10, B10) XA70R (A5, B5, A10, B10) A98J2 (7) A99T1 (3)
12VDC (Regulated) Origin: XA80 (A9-10, B9-10)	XA1 (A7, B7) XA2 (A6, B6) XA4 (A6, B6) XA5 (A6, B6) XA10 (A6, B6) XA11 (A6, B6) XA15 (A6, B6) XA20 (A9, B9) XA21 (A9, B9) XA22 (A9, B9) XA30 (A6, B6)	XA31 (A6, B6) XA32 (A9, B9) XA40R (A6, B6) XA50L (A6, B6) XA50R (A6, B6) XA51 (A6, B6) XA53 (A6, B6) XA70L (A9, B9) XA70R (A9, B9) A99T1 (4)
+5VDC (Regulated) Origin: XA80 (A20-21, B20-21)	XA1 (A9, B9)* XA2 (A8, B8)* XA4 (A8, B8)* XA11 (A8, B8)* XA15 (A8, B8) XA21 (A11-12, B11-12) XA22 (A11-12, B11-12) XA30 (A8, B8) XA31 (A8, B8) XA32 (A11-12, B11-12) XA40L (A8, B8)	XA40R (A8, B8) XA50R (A8, B8) XA52 (A8, B8) XA53 (A8, B8) XA60L (A12, B12) XA60R (A12, B12) XA61 (A11-12, B11-12) XA70L (A11-12, B11-12) XA70R (A11-12, B11-12) A98J2 (6) A99T1 (2)
+15VDC (Regulated) Origin: A99U2	A99T1 (5) A1J2 (PROBE power)*	XA1 (A8)*
+23VDC (Unregulated) Origin: A99CR10/CR11	XA16 (A7, B7) XA80 (B11)	A99U2
−23VDC (Unregulated) Origin: A99CR9/CR12	XA80 (B16)	
+2.5VDC (Unregulated) Origin: XA80 (A11) Battery A80BT1 (V-BAT)	XA60L (A10)	

Note:

All pins marked (*) are "isolated voltages" having passed through Motherboard isolation transformer A99T1 (see schematic 24).





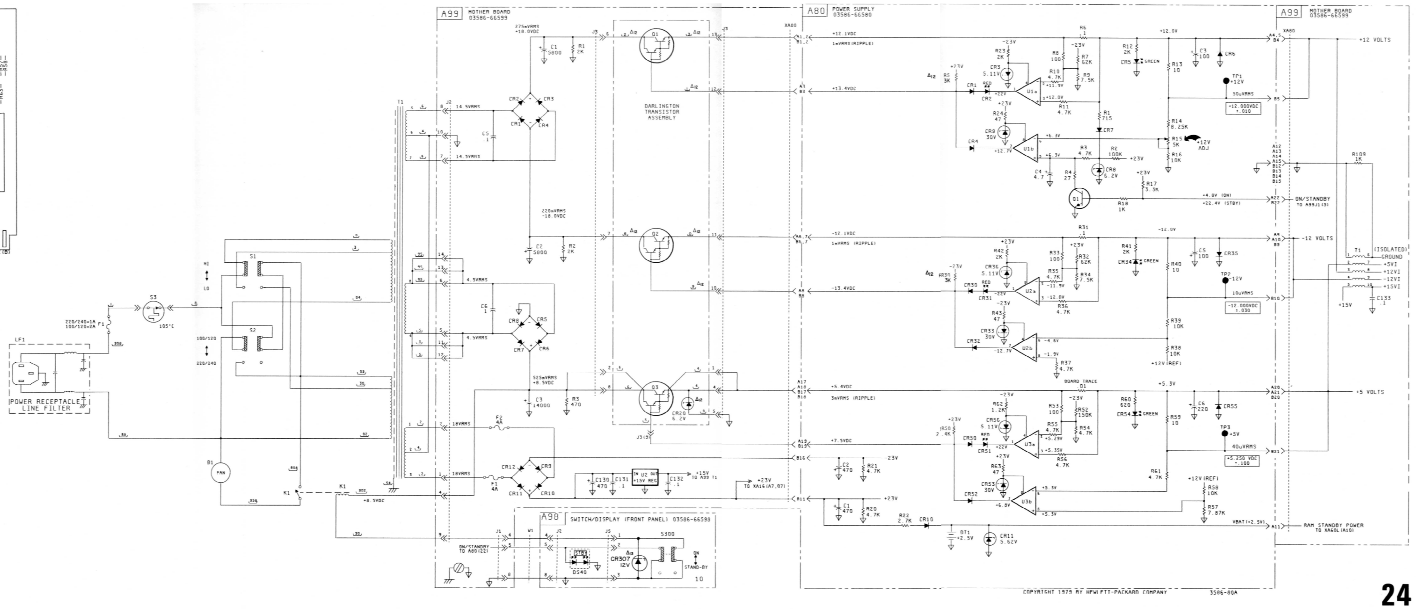


Figure 8-J-4. Schematic - Power Supply (A80/A99)
8-J-9/8-J-10

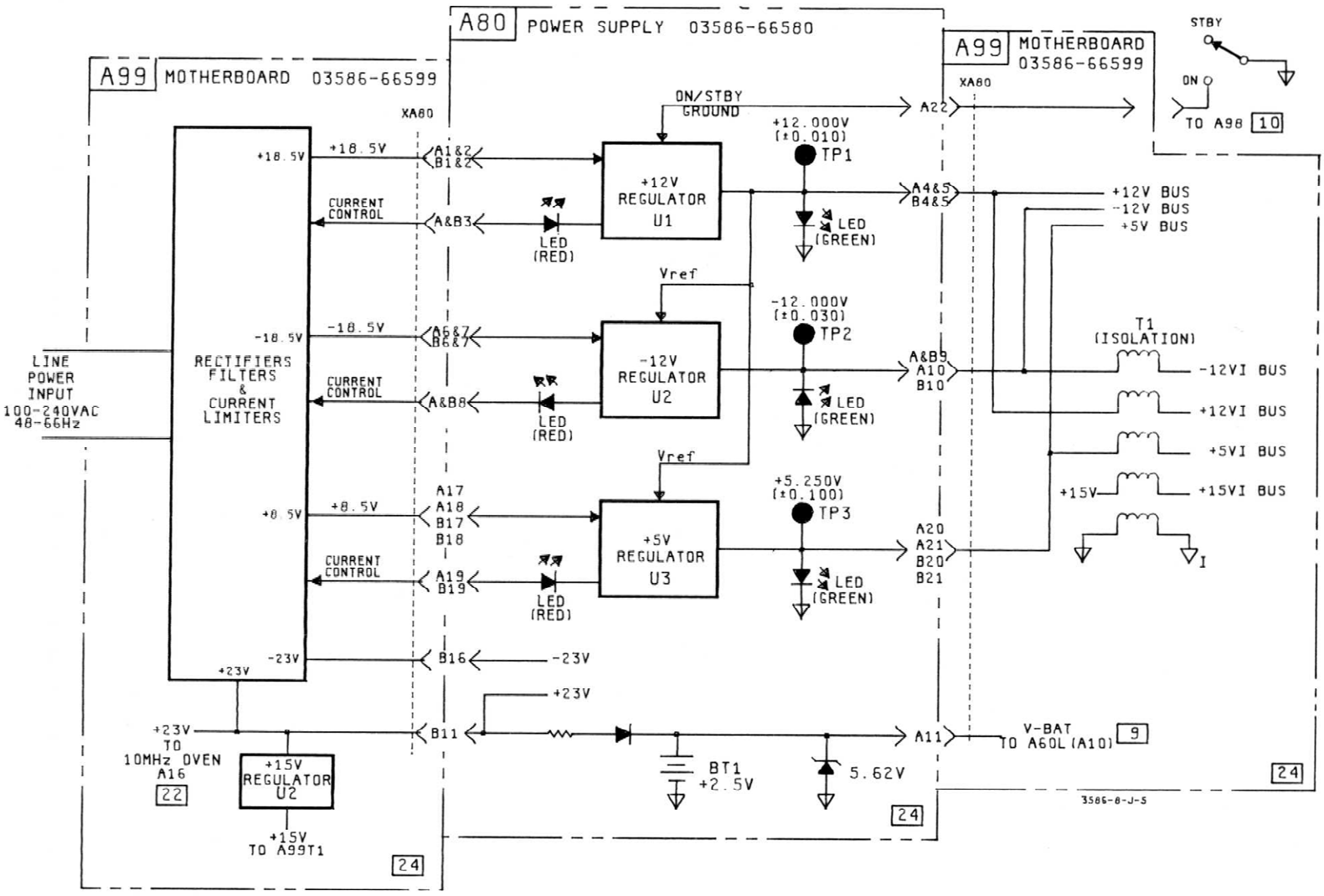


Figure 8-J-5. Functional Block - Power Supply (A80/A99)

This appendix contains a list of all mnemonics used throughout the service manual. It includes mnemonics associated with all PC boards and not just the Controller board. The list is compiled in alphabetical order for easy reference, with numbered mnemonics (e.g. 1Hz CLK) located at the end of the table.

Also included in this appendix are duplicate copies of the 3586 Major Signal Chart and Turn-on Troubleshooting Flowchart, along with a copy of the 3586 System Functional Block Diagram. Diagram.

Table 1. Mnemonic Dictionary.

Mnemonic	Description	Source
AØ-A15	Processor ADDRESS BUS lines.	A60U6
AD1-AD8	A/D Converter output. Pass six sequential BCD Words for level or frequency to A60 processor.	A22U6
AD CLK	A/D Clock. Gates serial AD DATA (DATA) from the processor to the A22 A/D Converter board.	A60U33(11)
AMP CLK	Amplifier Clock. Gates serial ISO DATA from the processor to the A2 Input Amplifier board. Goes through isolation transformer A99T5 enroute.	A60U34(3)
ANNUN 0-3	Annunciator 0-3. Latch lines for PAØ-PA7 data for four annunciator LED groups on the A98 Switch/Display board.	A60U30
API 1-5	Analog Phase Interpolator. These five lines control API current sinks on the A32 board.	A30U16
ATN	Attention. HP-IB control line.	A62J1
BBA	(H)BBA. Broadband Averaging. When HIGH, this line tells the A4 Detector/Logger circuit that AVE is on.	A2U4(2)
BBP LOG (RMS)	This line is the broadband power logarithmic DC signal from the A4 board to the A22 board.	A4U5(7)
BBP RF	Broadband Power RF. This line carries the total input spectra from the A2 board to the A4 BBP circuits.	A2Q12
BIAS	When HIGH, this line gates the Bias current on A30 into the Integrator.	A30U16(10)
BUS 0-7	HP-IB data bus lines to/from the A60 processor.	A61U23
CAL	(L) CAL. When LOW, shuts off the USB/LSB oscillators on A22 and tells the A15 and A21 boards that the instrument is in CAL or TF2 is active.	A22U2(9)
CAL OSC	Calibration Oscillator. 1.6625MHz (3586B) or 1.6425MHz (3586A) present only when option 003 is installed and either the CALibration cycle or TF2 (paragraph 8-58) are active.	A70U40(8)
COLD OVEN	Cold Oven. Tells the A60 processor (when HIGH) that the 10MHz Frequency Reference is not warmed up.	A16Q3
$\overline{\text{CS 2}}$	$\overline{\text{Chip Select 2}}$. Enable line to the PIA (A60U18).	A60U26(11)
DØ-D7	Processor DATA BUS lines.	A60U6
DATA	Serial control data to A21 (IF DATA), A22 (AD DATA), or A70 (OPT DATA).	A60U34(6)
DATA LATCH	Latch line for A/D DATA on the A22 A/D Converter board.	A60U30(13)
DAV	Data Valid. HP-IB control line.	A62J1
DIO1-DIO8	Data Input/Output. HP-IB data bus lines.	A62J1
DSP CLK	Display Clock. Gates serial display data (DSPSI) onto the A98 Switch/Display board.	A60U31(15)
DONE	(H) Done. Tells the A60 processor to scan the A/D Counter (A22U6) for six BCD data words representing level or frequency.	A22U12(6)
DSPSI	Display Serial Input. Serial display data to the A98 Switch/Display board for selection of 7-segment LED's and Key LED's.	A60U18(14)
E	Phase 2 clock line to the PIA.	A60U4(6)
EOI	End Or Identify. HP-IB control line.	A62J1

Table 1. Mnemonic Dictionary (Cont'd)

Mnemonic	Description	Source
F1-F20	Divide-by-N code lines to the A50 Step loop.	A60U22
FDC	Fractional-N Data Clock. Gates data or instruction words (FN1-FN8) onto the A30 FN ÷ N board.	A60U32(8)
FIV	Fractional-N Instruction Valid. Identifies FN1-FN8 as instruction (H) or as data (L).	A60U32(10)
FN1-FN8	Fractional-N Instruction or Data words to the A30 FN÷N board.	A60U35
FN UNLOCK	Tells the A60 processor that the Fractional-N VCO (A31) is unlocked.	A31Q9
IFC	Interface Clear. HP-IB control line.	A62J1
IF CLK	IF clock. Gates IF DATA (DATA) onto the A21 IF Gain/Detection board.	A60U33(6)
IMPØ-3	Impulse 0-3. A70 Impulse counter output to the A60 processor.	A70U21
INT	Interrupt, HP-IB Interrupt Request to the A60 processor (U6) via the IRQ output of the PIA (U18).	A61U22(9)
$\overline{\text{IRQ}}$	Interrupt Request. When LOW, tells the A60 processor that either the Display timer (U20) or the HP-IB has generated an interrupt.	A60U18(38)
ISO DATA	Isolated Data. Serial data to either A1 or A2 that goes through photo-isolator A99U1 enroute.	A60U34(11)
ISO LATCH	Latch line for ISO DATA. Goes through isolation transformer A 9 9 T 3 enroute to A1 or A2.	A60U32(4)
JITTER INVALID	Tells the A60 processor (when LOW) that the Frequency of the tone present on A70 for phase jitter measurements is not between 960Hz and 1060Hz.	A70U26(2)
ϕ JITTER (DC)	This line is the DC voltage representing Phase Jitter in degrees (peak-to-peak) from the A70 board to the A22 board.	A70U30(1)
KEY 0-7	Keyboard switch lines to the A60 processor.	A98U14
LISTEN	HP-IB control line identifying HP-IB "LISTEN" mode (when HIGH) to the A60 processor.	A61U22(16)
LLCAL	When HIGH, this line selects low-level CAL (−40dBm) from A4. When LOW, it selects high-level CAL (−20dBm).	A2U3(12)
LOAD BUS	Latch line for loading PAØ-PA7 data onto the A61 HP-IB processor BUS.	A60U30(15)
LOG INPUT	This line is the IF logarithmic DC signal from the A21 board (IF LOG) to the A22 A/D Converter.	A21U10(6)
LOG IN (WTD)	This line is the weighted audio logarithmic DC signal from the A70 board to the A22 board.	A70U10(1)
NEUTRAL	Common return line (isolated) for the OVERLOAD/UNDERLOAD lines to the A60 processor.	XA4(B13)
NDAC	Not Data Accepted. HP-IB control line.	A62J1
NRFD	Not Ready For Data. HP-IB control line.	A62J1
OPT CLK	Option Clock. Gates OPT DATA (DATA) onto the A70 Impairments board (Option 003).	A60U33(8)
OVERLOAD	Tells the A60 processor (when HIGH) that the BBP RF level is too high for the present A2 board RF Gain configuration. (Autorange situation.)	A4U6(7)

Table 1. Mnemonic Dictionary (Cont'd)

Mnemonic	Description	Source
PAØ-PA7	Controller output data lines (U18 Port A).	A60U1
R/T	Remote/Track. HP-IB mode switch on A62 controls this line.	A62S1
R/$\overline{W}$	Read/$\overline{Write}$. When HIGH, enables a READ operation of data into the processor. When LOW, processor writes onto the DATA Bus.	A60U6(34)
REF UNLK	Reference Unlocked. Tells the A60 processor (when LOW) that the A40 Frequency Reference oscillator is unlocked.	A40Q54
REMOTE	Tells the A60 processor (when HIGH) that the REN line on the HP-IB bus is true.	A61U22(15)
REN	Remote Enable. HP-IB control line.	A62J1
$\overline{RESET}$	At turn-on, and for +5V supply malfunctions, this line transitions from LOW to HIGH. This transition resets the A60 processor (U6), the PIA (U18) and the HP-IB processor (A61U1).	A60U5(14)
$\overline{S}$	Enable line to the Input Multiplexers.	A60U25(6)
SCAN	(H)SCAN. When the A/D Converter sets (H) DONE, the A60 processor outputs a six pulse sequence over (H) SCAN to sample six BCD data words from the A/D Counter (A22U6).	A60U18(15)
S + H	Sample/Hold. When HIGH, tells the A32 board to sample the Integrator output voltage. When LOW, tells A32 to hold its output to the A31 VCO (FN TUNE) constant.	A30U16(11)
SMOOTH	(H)SMOOTH. When HIGH, tells the A21 and A70 boards that AVEraging is on.	A22U2(5)
SRQ	Service Request. When HIGH, tells the A60 processor that the A61 processor has set the SRQ line on the HP-IB bus to true.	A61U22(12)
SSB DEMOD	Single Sideband Demodulated (audio).	A21U17(7)
SSB LO	Single Sideband Local Oscillator. This line carries the LSB or USB oscillator signal (or the A70 CAL OSC signal) to the A21 board to demodulate the 3586 input signal.	A22U102(13)
START	(L)START. When LOW, tells the A22 board to start the A/D Conversion process.	A60U30(14)
STEP UNLK	Step Unlocked. When LOW, tells the A60 processor that the Step loop is unlocked.	A50Q70
SUM UNLK	Sum Unlocked. When LOW, tells the A60 processor that the Sum loop is unlocked.	A53U4(2)
TALK	HP-IB control line that identifies the HP-IB "TALK" mode (when HIGH) to the A60 processor.	A61U22(19)
T CAL	Tracking Calibrator. This line (when LOW) turns on the Tracking CAL signal on the A4 board and energizes A2K1 to switch in the CAL signal.	A2U3(10)
T CLK	Termination Clock. Gates ISO DATA to the A1 board to make input termination impedance selections. Passes through isolation transformer A99T4 enroute to A1.	A60U34(8)
THRESH 1 THRESH 2	Threshold 1/2. These lines set the trip point reference for UL/OL on the A4 board.	A2U4
UNDERLOAD	Tells the A60 processor (when HIGH) that the BBP RF level is too low for the present A2 board RF gain configuration. (Autorange situation.)	A4U6(1)
V BAT	Standby battery voltage (+2.5V) for CMOS RAM memory protection.	A80BT1

Table 1. Mnemonic Dictionary (Cont'd)

Mnemonic	Description	Source
1Hz CLK	1Hz Clock. Used by A60 processor as one second timer for Impulse noise measurements.	A22U14(13)
1MHz EN	1MHz Enable. When LOW, gates the 1MHz calibration signal (TF12 - paragraph 8-79) through the A15 board.	A22U2(2)
2ND LO UNLOCK	Second L.O. Unlocked. When LOW, tells the A60 processor that the Second LO is unlocked.	A11U90(1)
35/10	(L)35/(H)10. When LOW, this line sets the gain of the A20 output amplifier at 35dB. When HIGH, the gain is 10dB.	A21U2(12)
400	(H)400. When HIGH, this line selects the 400Hz bandwidth on the A20 board. When LOW, it selects the 20Hz bandwidth.	A21U2(2)
3100/2000/1740 FILTER	When HIGH, this line selects the widest 3586 bandwidth from the A20 board. When LOW, the 400Hz or 20Hz bandwidth is selected.	A21U2(9)

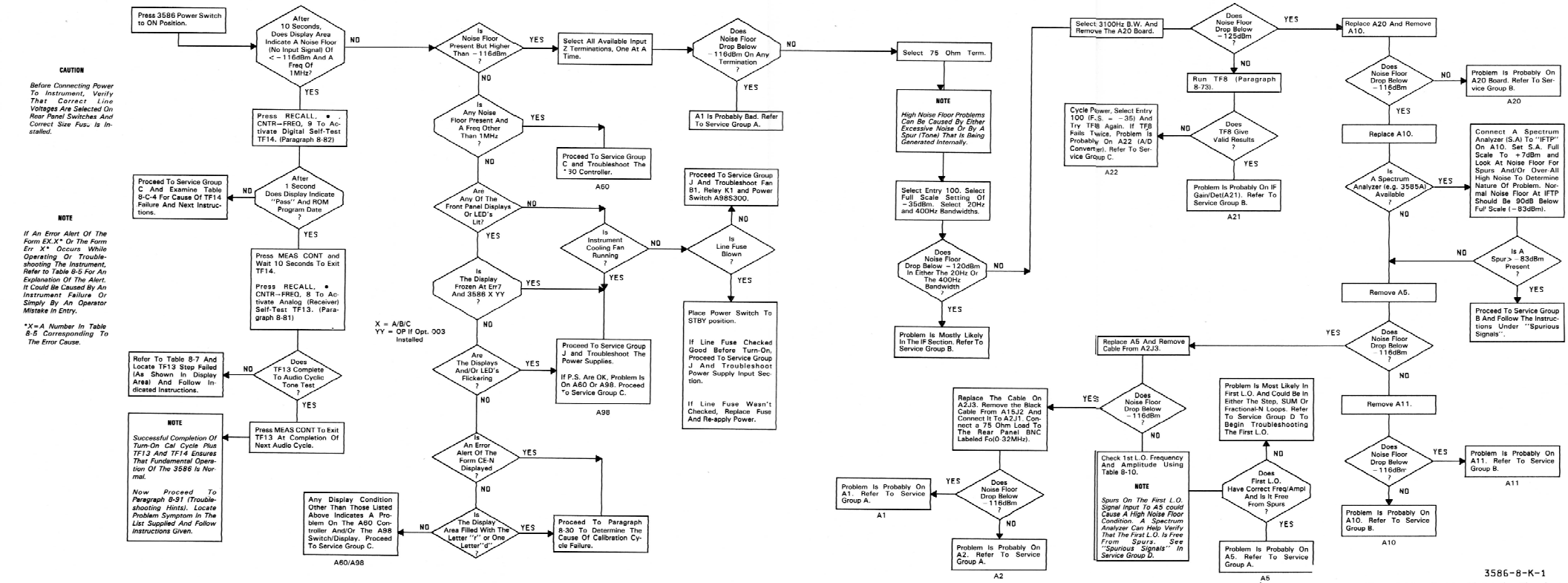
Table 2. Major Signal Chart.

Signal	Location	Frequency*	Level*#	SG	Remarks
10 MHz OVEN (Option 004-A16)	Rear Panel	10 MHz (± 1 Hz)	3.5 volts	H	Sine wave (Jumper removed)
10 MHz (Reference)	Rear Panel	10 MHz (± 2 Hz)	2.5 volts	H	Sine wave
50 MHz (Reference)	Test Jack on A40 (J6)	50 MHz (± 10 Hz)	1.2 volts	H	Sine wave
2 MHz (Reference) NNI	Test Jack on A40 (J2)	2 MHz (± 1 Hz)	900 mV	H	Square wave-narrow width-positive pulses.
50-82.5 MHz (First L.O.)	Test Jack on A51 (J2)	A 51 MHz (± 10 Hz) B 82 MHz (± 10 Hz)	A 700 mV B 750 mV	D/E	Sine wave-Tracks front panel frequency (+ 50 MHz).
54-86 MHz (Step Loop)	Test Jack on A50 (J2)	A 54 MHz (± 10 Hz) B 86 MHz (± 10 Hz)	A 700 mV B 750 mV	D	Sine wave-2 MHz steps.
20-40 MHz (FRAC N)	Test Jack on A31 (TP1)	A 30 MHz (± 10 Hz) B 40 MHz (± 10 Hz)	A 2.0 volts B 2.4 volts	E	Sine wave
0-32.5 MHz (Tracking Output)	Rear Panel (Fo)	0-32.5 MHz (± 10 Hz)	1.4 volts	F	Sine wave-Tracks front panel frequency.
49.984375 MHz (Second L.O.)	TP1 on A11	49.984375 MHz (± 2 Hz)	1.3 volts	B	Sine wave-(use extender board to get at TP1).
15.625 kHz (Second I.F.)	IF TP on A10	15.625 kHz (± 2 Hz)	1.4 volts	B	Sine wave

* Frequencies and levels indicated A are with 1,000,000 Hz selected on front panel.

Frequencies and levels indicated B are with 32,000,000 Hz selected on front panel.

\# All measurements were taken with a full scale signal of 1MHz at ØdBm present at the 75Ω input. 3586 set to ENTRY 100, Full Scale = ØdBm, LO DIST mode. Input signal levels taken with 3586 tuned to 1MHz. All levels are in volts (peak-peak).



3586-8-K-1

Figure 1. Turn-On Troubleshooting Flowchart

NOTES:

1. All measurements were taken with the 3586 tuned to 1MHz, ENTRY 100* selected, Full Scale setting = 0dBm, LO DIST mode. A full scale signal of 0dBm at 1MHz was present at the 75Ω input for all measurements.
2. A high impedance 10:1 scope probe was used.

*See paragraph 8-25 for selecting ENTRY 100.

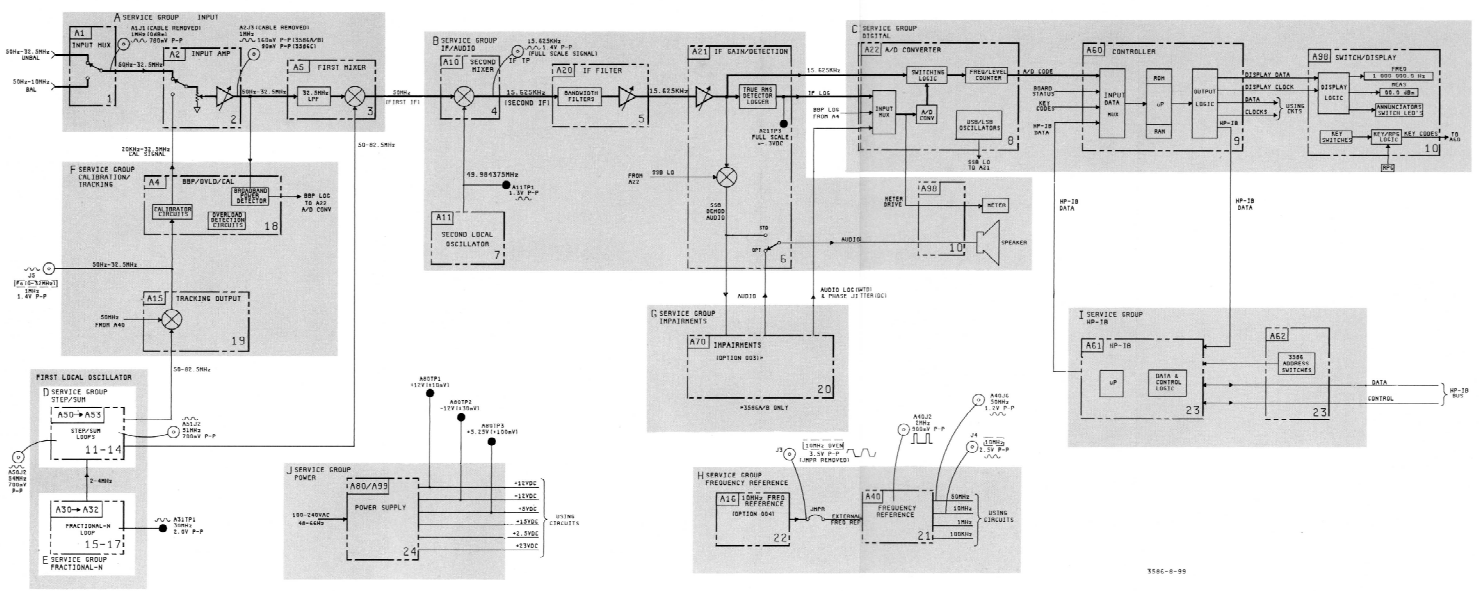


Figure 2. 3586 System Functional Block Diagram